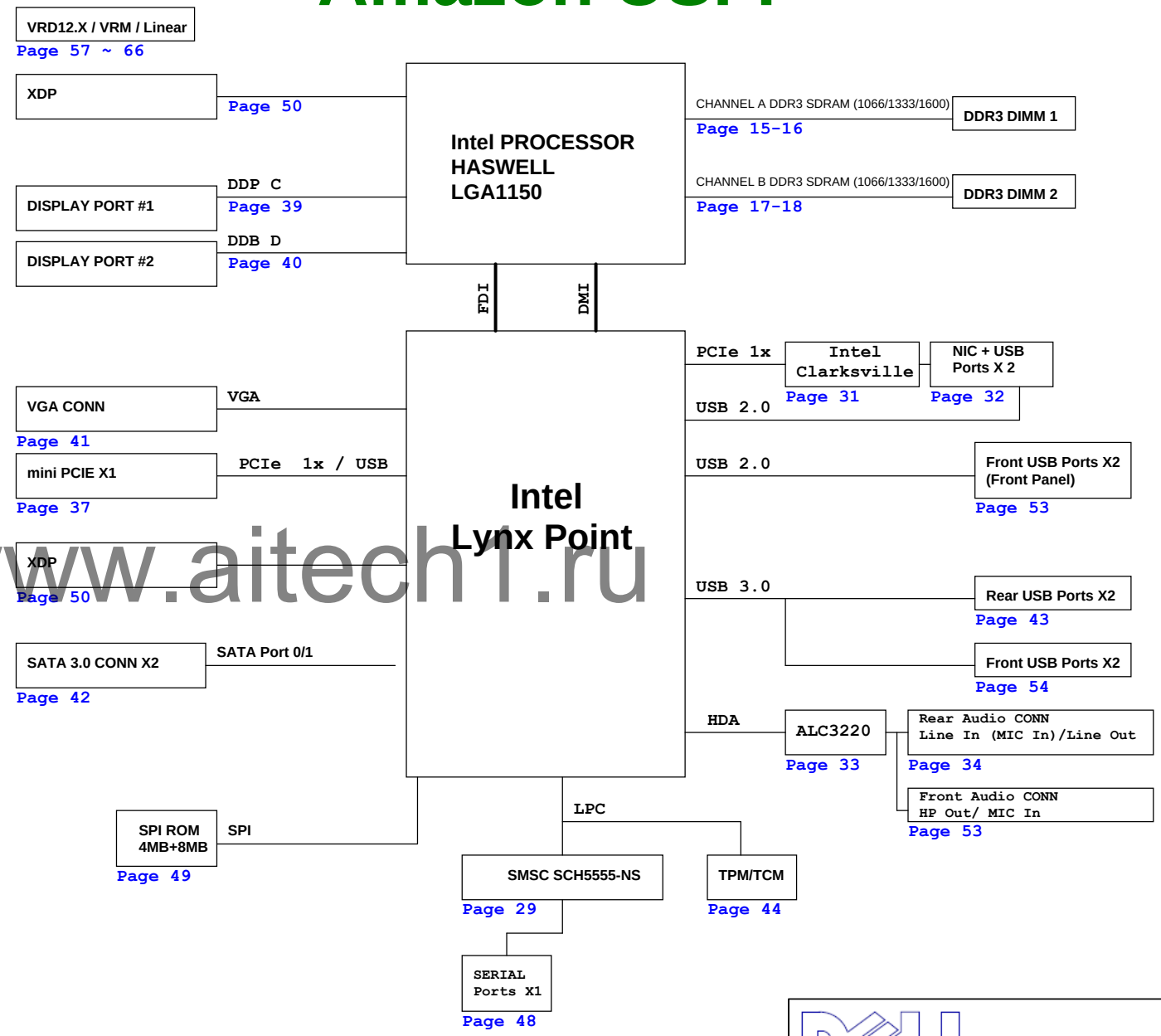
Amazon USFF



DESIGN	CHECK	APPROVE
Steven	Sam	Sdiu

DELL INC.

Title: **Index / Block diagram**

DWG NO: *Amazon USFF* Rev: A00

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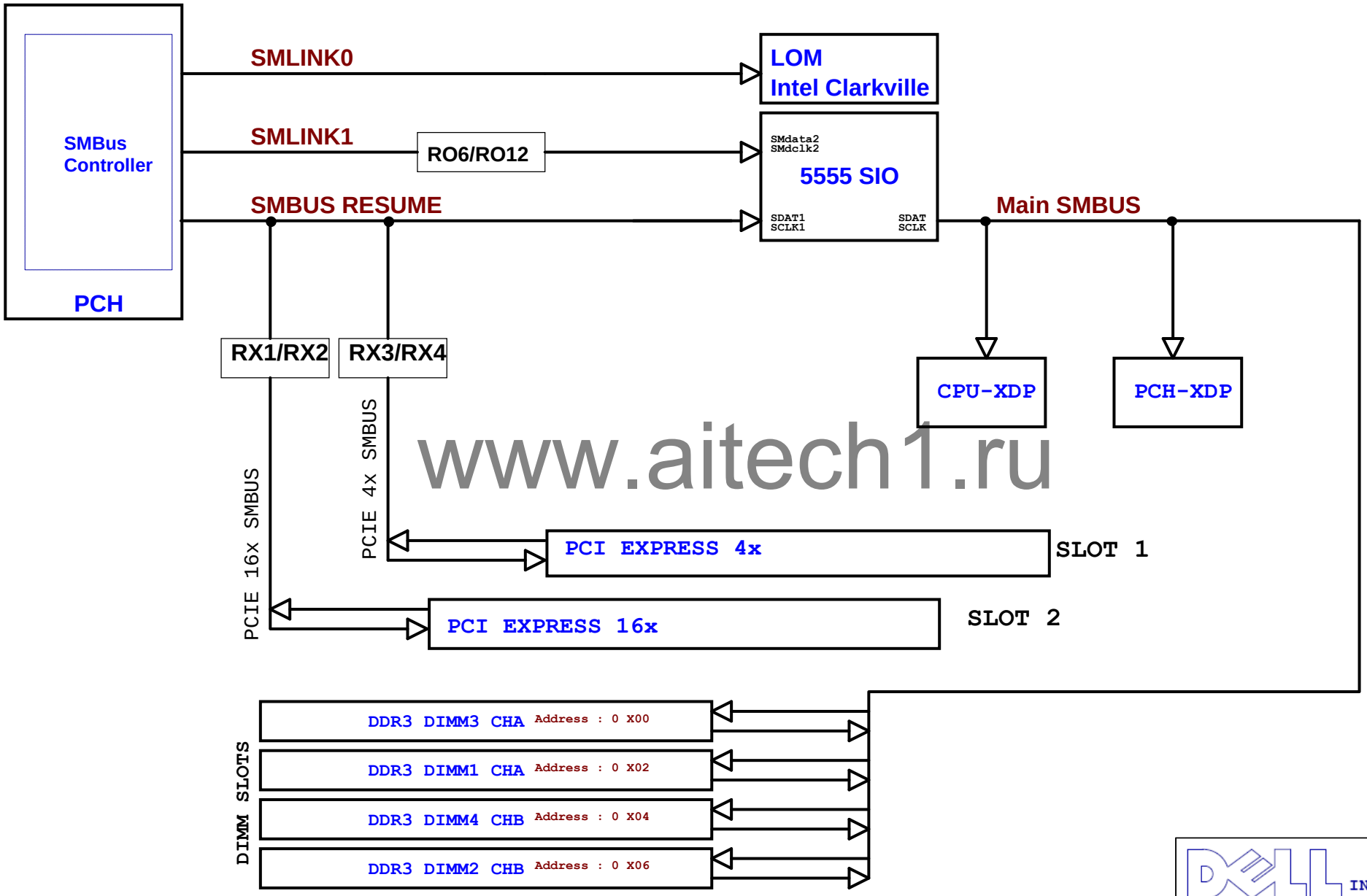
SMBUS DIAGRAM



DELL INC.

Title: BLOCK DIAGRAM

DWG NO: Amazon USFF

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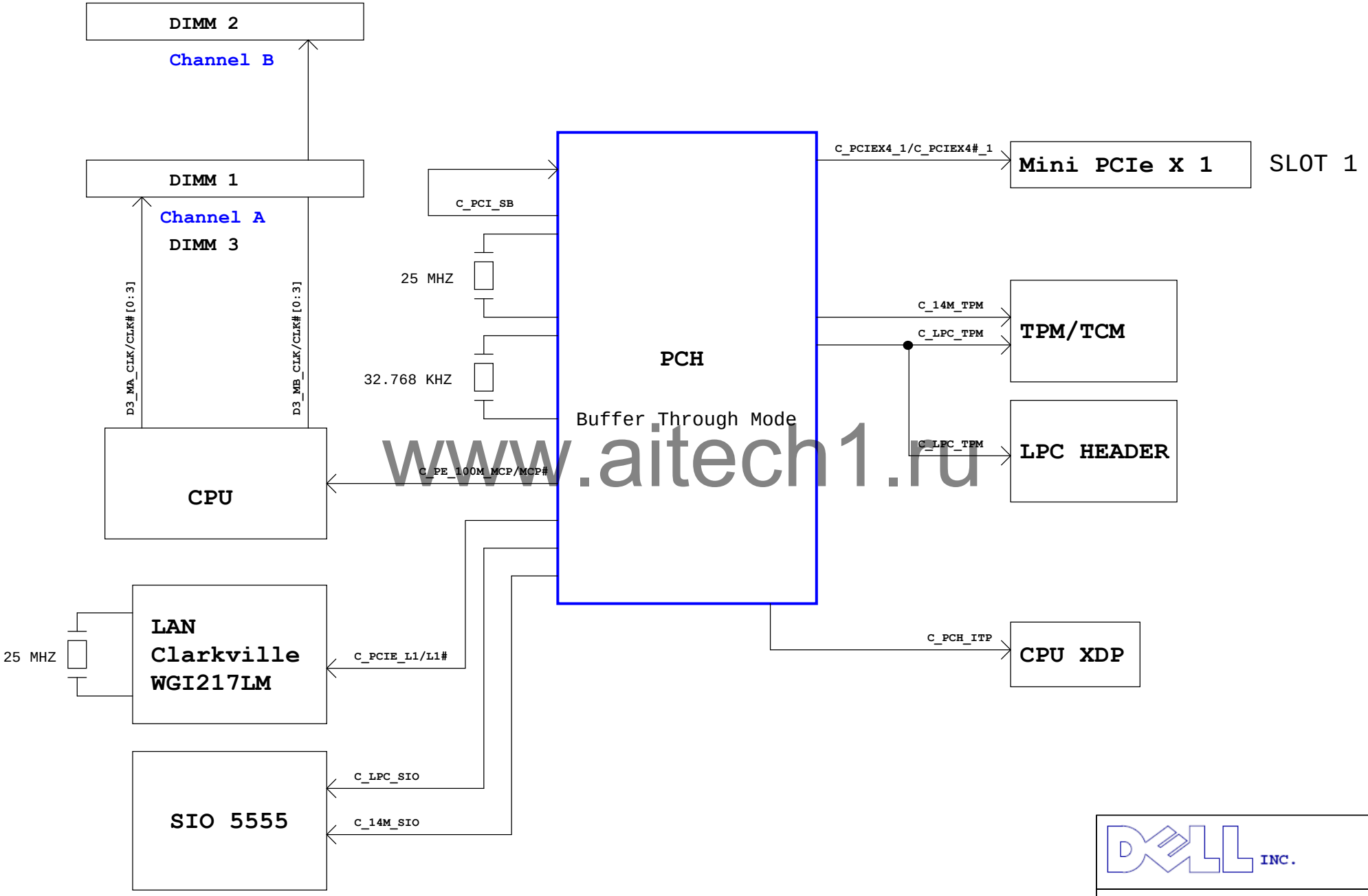

DELL INC.

Title: Clock Distribution

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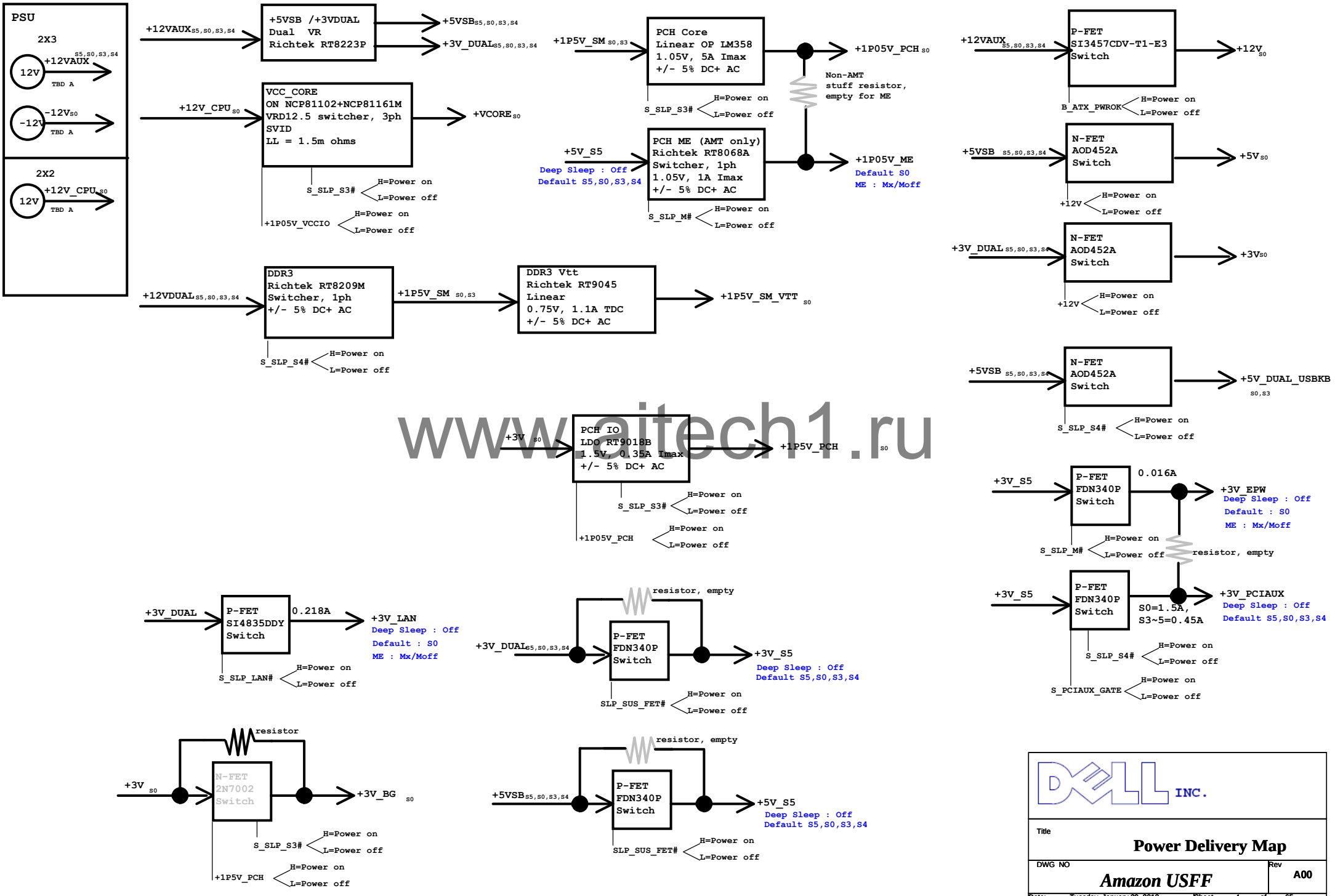
POWER DELIVERY MAP



DELL INC.

Title: **Power Delivery Map**

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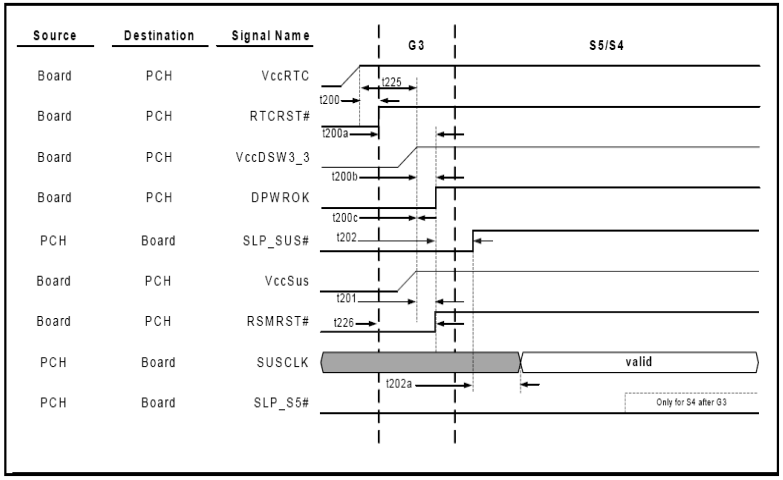
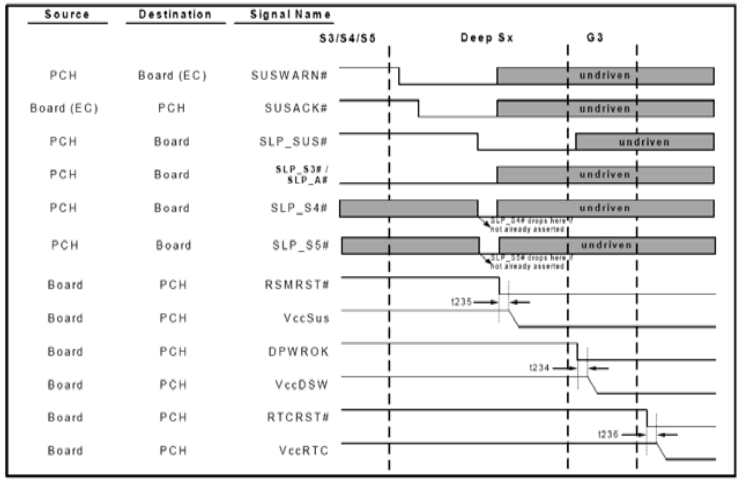
POWER ON Timing Diagram

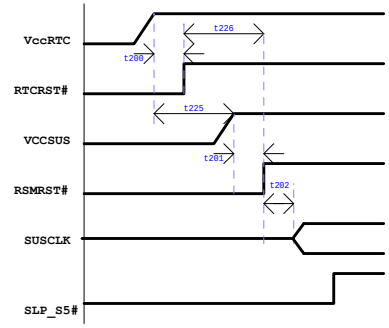
G3 --> S4/S5 (with Deep Sleep support)



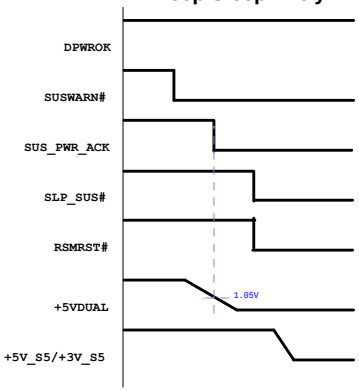
Sx --> Deep S4/S5 -->G3



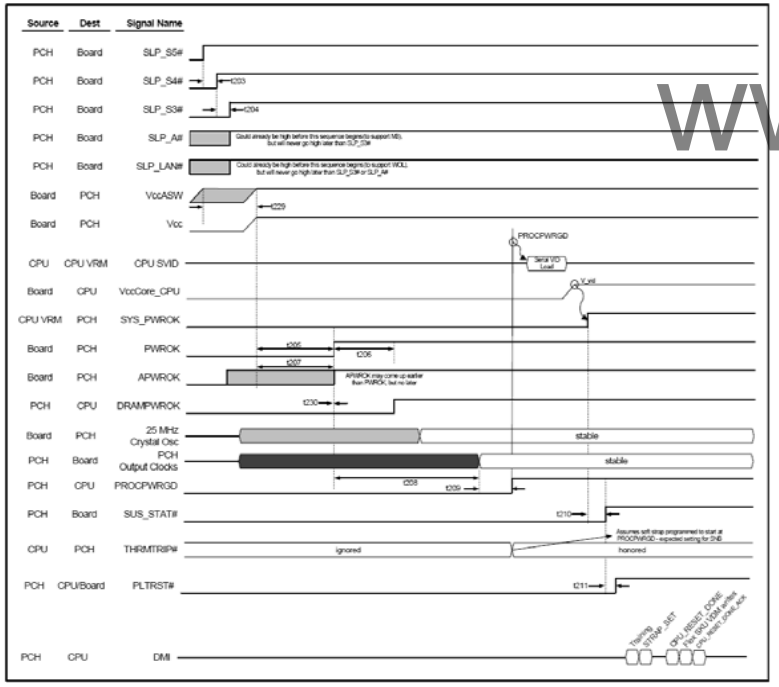
G3 to S4/S5 Timing Diagram



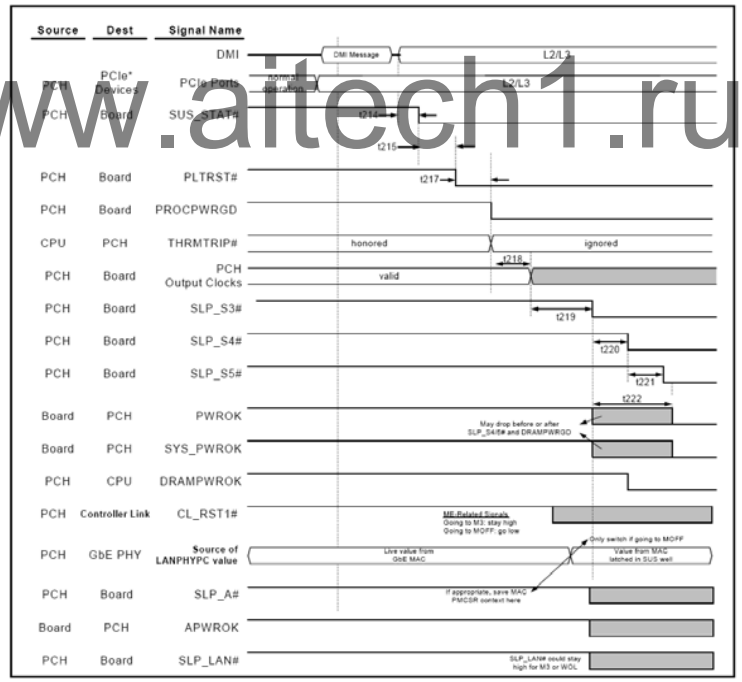
Deep Sleep Entry



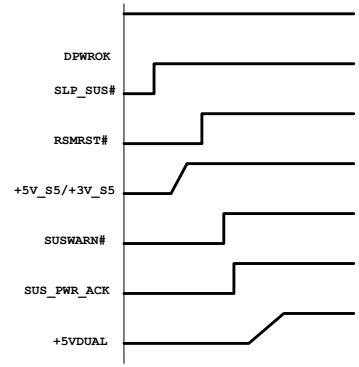
S5 --> S0



S0 --> S5



Deep Sleep Exit



DELL INC.

Title: **Power On Sequence**

DWG NO: *Amazon USFF*

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RESET / Power Good MAP

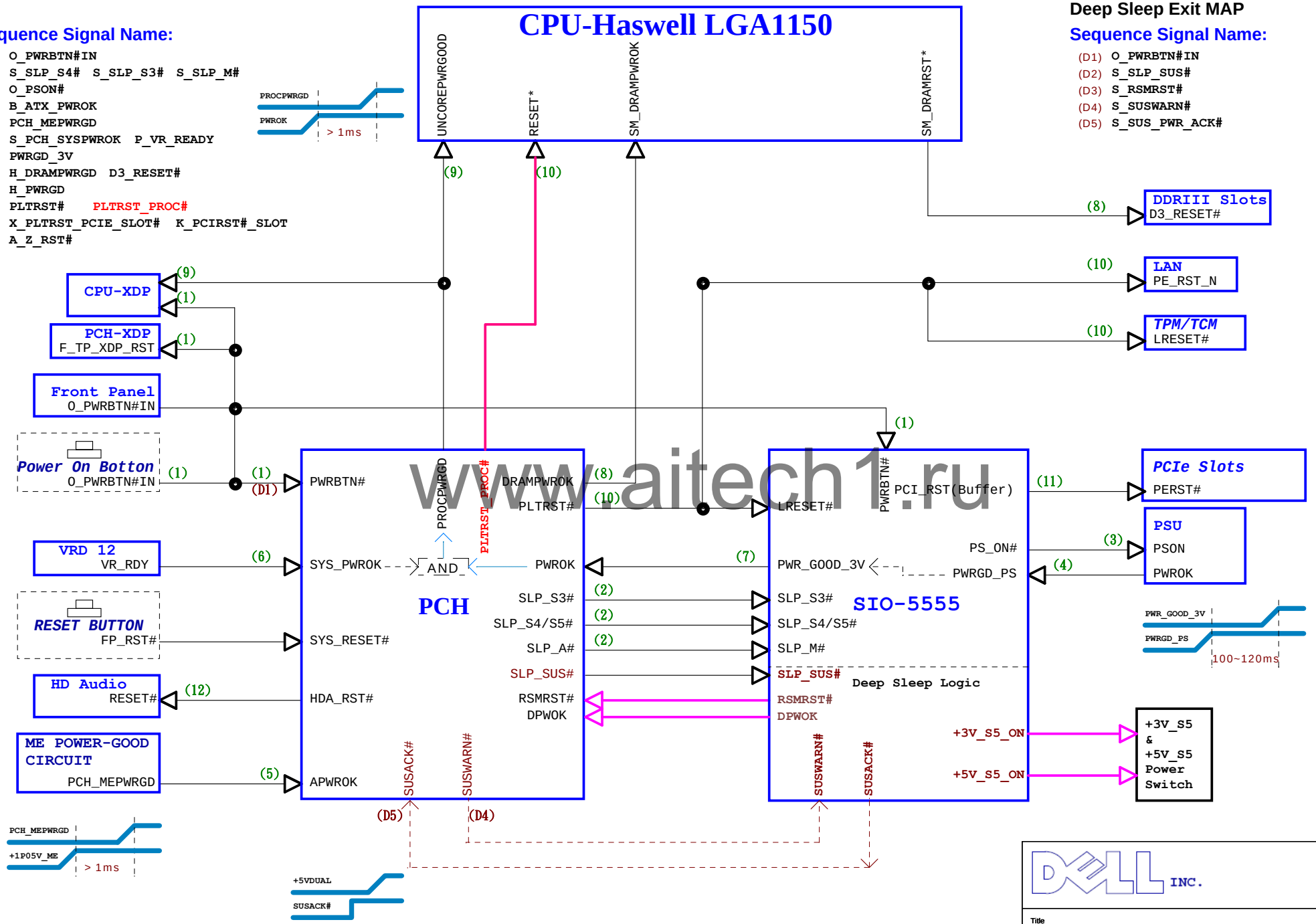
Sequence Signal Name:

(1) O_PWRBTN#IN
(2) S_SLP_S4# S_SLP_S3# S_SLP_M#
(3) O_PSON#
(4) B_ATX_PWROK
(5) PCH_MEPWRGD
(6) S_PCH_SYSPWROK P_VR_READY
(7) PWRGD_3V
(8) H_DRAMPWRGD D3_RESET#
(9) H_PWRGD
(10) PLTRST# PLTRST_PROC#
(11) X_PLTRST_PCIE_SLOT# K_PCIRST#_SLOT
(12) A_Z_RST#

Deep Sleep Exit MAP

Sequence Signal Name:

(D1) O_PWRBTN#IN
(D2) S_SLP_SUS#
(D3) S_RSMRST#
(D4) S_SUSWARN#
(D5) S_SUS_PWR_ACK#



DELL INC.

Title: Reset / Power Good Map

DWG NO: Amazon USFF

Rev: A00

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STRAPPING Table

PCH side

Table 36-18. Strapping Signals (Sheet 1 of 2)

Name	Type	Recommendations	Reason/Impact
SPKR	I	**Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2k-10k Ohm weak pull-up resistor.	
INIT3_3V#	I	Do not pull low.	
GPIO55	I/O	**Default Mode:** Internal pull-up. **Top Block Swap Mode:** Connect to ground with 4.7k Ohm weak pull-down resistor.	
SATA1GP/ GPIO19, GPIO51	I/O	**Default (SPI)** Left both SATA1GP/GPIO19 and GPIO51 floating. No pull up required. **Boot from PCI** Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor. Leave GPIO51 Floating. **Boot from LPC** Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.	If LPC is selected BIOS may still be placed on LPC, but all platforms with PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.
GPIO53	I/O	Do not pull low. Connect to ground with 1k Ohm pull-down resistor.	ESI strap for server platform ONLY
HDA_SDO	I/O	**Default** Do not pull high. **Disable ME in Manufacturing Mode** Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.	Flash descriptor Override
SPI_MOSI	I/O	Internal weak pull down.Do not pull high.	DMI RX Termination Voltage
SAAT3GP/ GPIO37	I/O	**Enable TLS:** Pull up with 1k Ohm to VccSus3.3. **Default (Disable TLS):** Leave NC. Internal pull down.	TLS confidentiality
GPIO8	I/O	Internal weak pull up.Do not pull low.	

Table 36-18. Strapping Signals (Sheet 2 of 2)

Name	Type	Recommendations	Reason/Impact
GPIO62/ SUSCLK	I/O	Internal weak pull up. Do not pull low.	On die PLL voltage regulator
GPIO36	I/O	Internal weak pull down. Do not pull high.	
DDPB_CTRL _DATA DDPC_CTRL _DATA DDPD_CTRL _DATA		Straps for digital ports B, C and D. For DisplayPort* - Should be pulled to 3.3V through a 2.2K ohms resistor to configure digital port. For DVI/HDMI configuration, the signal should be routed through the level shifter to the display connector. The signal is pulled to 3V before the level shifter and 5V before the display connector through a 2.2k ohms resistor. This signal should always be routed longer than SDVO/ DDPC_CTRLCLK by an inch. For DVI/HDMI configuration with the Cost Reduced level shifter, the signal should be routed through the pass gate sourced from 3.3V voltage to the display connector. The signal is pulled to 3V before the pass gate and 5V before the display connector through a 2.2k ohmsresistor. This signal should always be routed longer than SDVO/DDPC_CTRLCLK by an inch.	

CPU side

Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. • **CFG[1:0]:** Reserved configuration lane. A test point may be placed on the board for this lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal – x1 = Normal operation – x0 = Lane numbers reversed. • **CFG[3]:** PCI Express* Static x4 Lane Numbering Reversal – x1 = Normal operation – x0 = Lane numbers reversed • **CFG[4]:** Reserved configuration lane. A test point may be placed on the board for this lane. • **CFG[6:5]: PCI Express* Bifurcation:** – x00 = 1 x8, 2 x4 PCI Express* – x01 = reserved – x10 = 2 x8 PCI Express* – x11 = 1 x16 PCI Express* • **CFG[19:7]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I CMOS

Strapping Options Flash

GNT1#	SATA1GP/GPIO19	Routing
0	0	Flash Cycles Routed to LPC
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to SPI

Table 34-6. PCH Digital Display Strapping Signals

Checklist Item	Recommendations	Direction	Comments
DDPx_CTRLDATA	Straps for digital port B, C and D. For DisplayPort* - Should be pulled to 3.3V through a 2.2K W resistor to configure digital port. For DVI/HDMI configuration, the signal should be routed through the level shifter to the display connector. The signal is pulled to 3V before the level shifter and 5V before the display connector through a 2.2KW resistor. This signal should always be routed longer than DDPC_CTRLCLK by an inch. For DVI/HDMI configuration with the Cost Reduced level shifter, the signal should be routed through the pass gate sourced from 3.3V voltage. The signal is pulled to 3V before the pass gate and 5V before the display connector through a 2.2KW resistor and a Schottky diode. This signal should always be routed longer than DDPC_CTRLCLK by an inch. Also ensure schottky diode is not shared with DDPC_CTRLCLK.	BI	

SIO SMSC5555

PIN NAME	NET		Strapping description
GP070 / PWM4 (PIN127)	O_SPEAKER	1	Diag_En Disable
		0	Diag_En Enable DEFAULT

DELL INC.

Title: **GPIO/IRQ/IDSEL Table**

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PIN OUT	Power well	Bufffer Type	Signal Name	EX-PU/PD	*Current Usage I/O/NU/Native/Strapping	Programming Function
4	V3_S5	IO4	NC	NA	Native	NA
5	V3_S5	IO4	NC	NA	Native	NA
7	V3_S5	IO4	NC	NA	Native	NA
8	V3_S5	IO4	NC	NA	Native	NA
70	V3_S5	IO4	S_SUSWARN#	NA	Native	NA
22	V3_S5	IO4	O_PECI_REG#	10k pull-up to +3V	Native	NA
25	V3_S5	IO8	O_YELLOW#	499 pull-up to +5V_S5	Native	NA
26	V3_S5	IO8	O_GREEN#	499 pull-up to +5V_S5	Native	NA
27	V3_S5	IO8	S_SML1DATA	2.2k pull-up to +3V_S5	Native	NA
28	V3_S5	IO8	S_SML1CLK	2.2k pull-up to +3V_S5	Native	NA
30	V3_S5	IO4	O_DPWROK	10k pull-down to GND	Native	NA
35	V3_S5	IO4	TMIN_SHIFT	8.2k pull-up to +3V_S5 330k pull-down to GND (Dummy)	I	1 : default 0 : Tmin down adjustment
36	V3_S5	IO4	O_PWRBTN#IN	1k pull-up to +3V_DUAL (Dummy)	Native	NA
38	V3_S5	LVI0D24	H_PROCHOT#	51ohm pull-up to H_CPU_VCCIO_R10HT	Native	NA
39	V3_S5	IO4	O_SEN_CPUFAN	1k pull-up to +3V	Native	NA
40	V3_S5	IO4	O_SEN_CHAFAN	1k pull-up to +3V	Native	NA
41	V3_S5	IO4	NC	NA	NU	NA
49	V3_S5	IO4	O_CPUFAN_PWM	4.7k pull-up to +3V	Native	NA
50	V3_S5	IO4	O_CHAFAN_PWM	4.7k pull-up to +3V	Native	NA
51	V3_S5	IO4	NC	NA	NU	NA
52	V3_S5	IO4	O_FP_CBL_DET#	8.2k pull-up to +3V_S5	I	1 : default 0 : power switch cable plugged
53	V3_S5	IO4	X_PLTRST_PCIE_SLOT#	NA	Native	NA
54	V3_S5	IO4	NC	NA	NU	NA
55	V3_S5	OD4	O_PSON#	4.7k pull-up to +5VSB	Native	NA
56	V3_S5	IO4	O_AUD_PCSPKR_DET#	8.2k pull-up to +3V_S5	I	1 : default 0 : PC speaker cable plugged
58	V3_S5	IO4	O_SUS_3V_F_ON	NA	Native	NA
59	V3_S5	IO4	PWRGD_3V	NA	Native	NA
60	V3_S5	O4	O_RSMRST#	NA	NU	NA
69	V3_S5	IO4	NC	NA	NU	NA
72	V3_S5	IO8	NC	NA	NU	NA
74	V3_S5	IO8	NC	NA	NU	NA
77	V3_S5	IO4	O_PME#	10k pull-up to +3V_S5	Native	NA
78	V3_S5	IO4	NC	NA	NU	NA
98	V3_S5	IO4	O_DCD1#_R	NA	Native	NA
99	V3_S5	IO4	O_DSR1#_R	NA	Native	NA
100	V3_S5	IO4	O_RID1_R	NA	Native	NA
101	V3_S5	IO4	O_RTS1#_R	10k pull-up to +3V	Native	NA
102	V3_S5	IO8	O_TID1_R_C	10k pull-up to +3V	Native	NA
103	V3_S5	IO4	O_CTS1#_R	NA	Native	NA
104	V3_S5	IO4	O_DTR1#_R	NA	Native	NA
105	V3_S5	IO4	O_RI1#_R	NA	Native	NA
107	V3_S5	IO4	NC	NA	Native	NA
108	V3_S5	IO4	NC	NA	Native	NA
109	V3_S5	IO4	NC	NA	Native	NA
110	V3_S5	IO4	O_PWR2_PRSNT	10k pull-up to +3V	Native	NA
111	V3_S5	IO8	O_MB_REG_PG	10k pull-up to +3V	Native	NA
112	V3_S5	IO4	NC	NA	Native	NA
113	V3_S5	IO4	O_MEM_REG_PG	10k pull-up to +3V	Native	NA
114	V3_S5	IO4	NC	NA	Native	NA
120	V3_S5	IO4	O_KB_RST#	10k pull-up to +3V	Native	NA
121	V3_S5	IO4	O_A20GATE	10k pull-up to +3V	Native	NA
124	V3_S5	IO4	S_SLP_S5#	NA	Native	NA
127	V3_S5	IO4	O_SPEAKER	8.2k pull-up to +3V_S5(dummy) 8.2k pull-down to GND	Native	NA
128	V3_S5	IO4	S_SLP_M#	NA	Native	NA
75	V3_S5	IO4	O_SUS_5VON	22k pull-up to +5VSB	Native	NA
76	V3_S5	IO4	O_SUS_3V_ON	NA	Native	NA
84	V3_S5	IO12	NC	NA	Native	NA
85	V3_S5	IO12	NC	NA	Native	NA
86	V3_S5	IO12	NC	NA	Native	NA
87	V3_S5	IO12	NC	NA	Native	NA
88	V3_S5	IO12	NC	NA	Native	NA
89	V3_S5	IO12	NC	NA	Native	NA
90	V3_S5	IO12	NC	NA	Native	NA
91	V3_S5	IO12	NC	NA	Native	NA
63	V3_S5	IO4	NC	NA	Native	NA
64	V3_S5	IO4	NC	NA	Native	NA
65	V3_S5	IO4	NC	NA	Native	NA
66	V3_S5	IO4	NC	NA	Native	NA
97	V3_S5	IO12	NC	NA	Native	NA
15	V3_S5	IO4	NC	NA	Native	NA
80	V3_S5	IO8	S_SMBDATA_RESUME	2.2k pull-up to +3V_S5	Native	NA
81	V3_S5	IO8	S_SMBDATA_MAIN	2.7k pull-up to +3V	Native	NA
82	V3_S5	IO8	S_SMBCLK_RESUME	2.2k pull-up to +3V_S5	Native	NA
83	V3_S5	IO8	S_SMBCLK_MAIN	2.7k pull-up to +3V	Native	NA
93	V3_S5	IO8	O_PCIAUX_CTRL	NA	Native	NA
94	V3_S5	IO8	O_PCIAUX_OATE	NA	NU	NA
95	V3_S5	IO4	NC	NA	Native	NA
96	V3_S5	IO12	O_SUS_ACK_EN#	NA	NU	NA

PCH GPIO Summary

GPIO	Mult Function Pin	PIN OUT	Type	Power Well	Default	Signal Name	IN-PU/PD	EX-PU/PD	*Current Usage
GPIO[0]	BMBUSY#/GPIO0	G38	I/O	Core	GPI	S_PECI_REG#	--	10k pull-up to +3V	I
GPIO[1]	TACH1/GPIO1	AT31	I/O	Core	GPI	S_GPI_CHASSIS_ID0	20K IN-PU (only on TACH1)	10k pull-up to +3V 1k pull-down to GND (dummy)	I
GPIO[2]	PIRQE#/GPIO2	AR30	I/OD	Core	GPI	PCIE_MINI_CPUSB_DETECT#	--	8.2k pull-up to +3V	I
GPIO[3]	PIRQF#/GPIO3	AV29	I/OD	Core	GPI	V_DDSP_C_HPD	--	--	I
GPIO[4]	PIRQG#/GPIO4	AV28	I/OD	Core	GPI	V_GPI_VGA_CBL_DET#	--	8.2k pull-up to +3V	I
GPIO[5]	PIRQH#/GPIO5	AT27	I/OD	Core	GPI	PCIE_MINI_CPPE_DETECT#	--	8.2k pull-up to +3V	I
GPIO[6]	TACH2/GPIO6	AM26	I/O	Core	GPI	S_GPIO6	20K IN-PU (only on TACH2)	10k pull-up to +3V	NU
GPIO[7]	TACH3/GPIO7	AV24	I/O	Core	GPI	S_GPI_SKU2	20K IN-PU (only on TACH3)	10k pull-up to +3V (dummy) 220 pull-down to GND	I
GPIO[8]	GPIO8	AC40	I/O	Suspend	GPO	S_IGC_EN_N	20K IN-PU	--	NU (connected to XDP_PCH)
GPIO[9]	OC5#/GPIO9	AC41	I/O	Suspend	Native	X_WLAN_WAKE#	--	8.2k pull-up to +3V_S5	I
GPIO[10]	OC6#/GPIO10	AF40	I/O	Suspend	Native	U_USB_OC_R_#6	--	--	Native
GPIO[11]	SMBALERT#/GPIO11	AO31	I/O	Suspend	Native	X4_WAKE#	--	10k pull-up to +3V_S5	NU
GPIO[12]	LAN_PHY_PWR_CTRL/GPIO12	AL40	I/O	Suspend	Native	L_LAN_DISABLE#	--	10k pull-up to +3V_LAN 10k pull-down to GND (dummy)	O
GPIO[13]	GPIO13	AN22	I/O	Suspend	GPI	S_GPIO13	--	10k pull-up to +3V_S5	NU
GPIO[14]	OC7#/GPIO14	AO40	I/O	Suspend	Native	U_USB_OC_R_#7	--	--	Native
GPIO[15]	GPIO15	AE34	I/O	Suspend	GPO	S_GPIO15	--	10k pull-up to +3V_S5	NU
GPIO[16]	SATA4GP/GPIO16	M39	I/O	Core	GPI	S_SATA4GP	--	10k pull-up to +3V 10k pull-down to GND (dummy)	Strapping
GPIO[17]	TACH0/GPIO17	AP28	I/O	Core	GPI	S_GPI_CHASSIS_ID1	20K IN-PU (only on TACH0)	10k pull-up to +3V 1k pull-down to GND(dummy)	I
GPIO[18]	PCIECLKRQ1#/GPIO18	P39	I/O	Core	Native	S_GPIO18	--	10k pull-up to +3V	NU (connected to XDP_PCH)
GPIO[19]	SATA1GP/GPIO19	J40	I/O	Core	GPI	S_SATA1GP	20K IN-PU	1k pull-up to +3V (dummy) 10k pull-down to GND (dummy)	Strapping
GPIO[20]	PCIECLKRQ2#/GPIO20	P37	I/O	Core	Native	S_SMI_N	--	10k pull-up to +3V 10k pull-down to GND (dummy)	NU (connected to XDP_PCH)
GPIO[21]	SATA0GP/GPIO21	M37	I/O	Core	GPI	S_GPI_BRD_REV0	--	10k pull-up to +3V (dummy) 10k pull-down to GND	I
GPIO[22]	ZCLOCK/GPIO22	L39	I/O	Core	GPI	H_PCH_CONFIG_JUMPER	--	1k pull-up to +3V 4.7k pull-down to GND (dummy)	NU
GPIO[23]	PCIDRQ1#/GPIO23	AP26	I/O	Core	Native	S_LDRQ1#	20K IN-PU	--	NU
GPIO[24]	GPIO24	AE34	I/O	Suspend	GPO	H_SKTOCC#	--	100k pull-up to +3V_S5	I
GPIO[25]	PCIECLKRQ3#/GPIO25	AA39	I/O	Suspend	Native	S_GPIO25	--	100k pull-up to +3V_S5	NU
GPIO[26]	PCIECLKRQ3#/GPIO26	W35	I/O	Suspend	Native	S_MFG_MODE_OR	--	10k pull-up to +3V_S5	O
GPIO[27]	GPIO27	AU34	I/O	Deep Sleep	GPI	L_LAN_WAKE_N	20K IN-PU	4.7k pull-up to +3V_DUAL	I
GPIO[28]	GPIO28	V41	I/O	Suspend	GPO	S_GPIO28	--	10k pull-up to +3V_S5	NU
GPIO[29]	SLP_WLAN#/GPIO29	AL39	I/O	Suspend	GPI	S_GPIO29	--	10k pull-up to +3V_S5	NU
GPIO[30]	SUSWARN#/SUSPWRDNACK/GPIO30	AG41	I/O	Suspend	Native	S_SUSWARN#	--	--	Native
GPIO[31]	GPIO31	AM36	I/O	Deep Sleep	GPI	S_PSWD_CLR	20K IN-PD	8.2k pull-up to +3V_DUAL	I
GPIO[32]	CLKRUN#/GPIO32	N32	I/O	Core	GPO	S_GPI_SKU0	--	10k pull-up to +3V (dummy) 220 pull-down to GND	I
GPIO[33]	HDA_DOCK_EN#/GPIO33	AV26	I/O	Core	GPO	S_GPIO33	PD	--	NU
GPIO[34]	GPIO34	N34	I/O	Core	GPI	S_GPIO34	--	10k pull-up to +3V	NU
GPIO[35]	GPIO35	M40	I/O	Core	GPO	S_GPI_SKU1	--	10k pull-up to +3V (dummy) 220 pull-down to GND	I
GPIO[36]	SATA2GP/GPIO36	H40	I/O	Core	GPI	S_GPIO36	20K IN-PD	1k pull-up to +3V (dummy) 10k pull-down to GND (dummy)	Strapping

GPIO	Mult Function Pin	PIN OUT	Type	Power Well	Default	Signal Name	IN-PU/PD	EX-PU/PD	*Current Usage
GPIO[37]	SATA3GP/GPIO37	N41	I/O	Core	GPI	S_GPIO37	20K IN-PD	1k pull-up to +3V 10k pull-down to GND (dummy)	Strapping
GPIO[38]	SLOAD/GPIO38	H41	I/O	Core	GPI	S_GPI_CHASSIS_ID2	--	10k pull-up to +3V (dummy) 10k pull-down to GND	I
GPIO[39]	SDATAOUT0/GPIO39	R31	I/O	Core	GPI	A_FP_PRES#	--	10k pull-up to +3V	I
GPIO[40]	OC1#/GPIO40	AF37	I/O	Suspend	Native	U_USB_OC_R_#1	--	8.2k pull-up to +3V_S5	NU
GPIO[41]	OC2#/GPIO41	AD39	I/O	Suspend	Native	U_USB_OC_R_#2	--		Native
GPIO[42]	OC3#/GPIO42	AD40	I/O	Suspend	Native	U_USB_OC_R_#3	--		Native
GPIO[43]	OC4#/GPIO43	AF39	I/O	Suspend	Native	U_USB_OC_R_#4	--		Native
GPIO[44]	PCIECLKRQ5#/GPIO44	AA36	I/O	Suspend	Native	S_INTRUD_CBL_DET#	20K IN-PU	10k pull-up to +3V_S5	I
GPIO[45]	PCIECLKRQ6#/GPIO45	W32	I/O	Suspend	Native	S_GPIO45	--	10k pull-up to +3V_S5	NU
GPIO[46]	PCIECLKRQ7#/GPIO46	AA40	I/O	Suspend	Native	S_GPI_BRD_REV1	20K IN-PU	10k pull-up to +3V_S5 (dummy) 1k pull-down to GND	I
GPIO[48]	SDATAOUT1/GPIO48	L40	I/O	Core	GPI	V_DDSP_B_HPD	--	--	I
GPIO[49]	SATA5GP/GPIO49	N40	I/O	Core	GPI	S_GPIO49	--	10k pull-up to +3V (dummy)	Strapping
GPIO[50]	GPIO50	AH26	I/O	Core	GPI	S_GPIO50	--	10k pull-up to +3V	NU
GPIO[51]	GPIO51	AU31	I/O	Core	GPO	S_GPIO51	20K IN-PU	1k pull-up to +3V (dummy) 10k pull-down to GND	Strapping
GPIO[52]	GPIO52	AJ26	I/O	Core	GPI	S_GPIO52	--	10k pull-up to +3V	NU
GPIO[53]	GPIO53	AV31	I/O	Core	GPO	S_GPIO53	20K IN-PU	1k pull-down to GND (dum	Strapping
GPIO[54]	GPIO54	AW33	I/O	Core	GPI	S_GPIO54	--	10k pull-up to +3V	NU
GPIO[55]	GPIO55	R30	I/O	Core	GPO	S_GPIO55	20K IN-PU	4.7k pull-down to GND (dumm	Strapping
GPIO[57]	GPIO57	AC36	I/O	Suspend	GPI	S_GPIO57	--	10k pull-up to +3V_S5	NU
GPIO[58]	SML1CLK/GPIO58	AK36	I/O	Suspend	Native	S_SML1CLK	--	2.2k pull-up to +3V_S5	Native
GPIO[59]	OC0#/GPIO59	AE40	I/O	Suspend	Native	U_USB_OC_R_#0	--	8.2k pull-up to +3V_S5	Native
GPIO[60]	SMLOALERT#/GPIO60	AG35	I/O	Suspend	Native	S_SMI0LALERT#	--	10k pull-up to +3V_S5	NU
GPIO[61]	SUS_STAT#/GPIO61	AD37	I/O	Suspend	Native	S_SUS_STAT#	--	10k pull-up to +3V_S5 (dummy	NU
GPIO[62]	SUSCLK/GPIO62	W36	I/O	Suspend	Native	S_SUSCLK_R	PU	--	Native
GPIO[63]	SLP_S5#/GPIO63	AA35	I/O	Suspend	Native	S_SLP_S5#	--	--	Native
GPIO[64]	CLKOUTFLEX0/GPIO64	AV8	I/O	Core	Native	S_TP_CLKOUTFLEX0	20K IN-PD	---	NU
GPIO[65]	CLKOUTFLEX1/GPIO65	AT9	I/O	Core	Native	C_14M_SIO_R	20K IN-PD	---	Native
GPIO[66]	CLKOUTFLEX2/GPIO66	AV9	I/O	Core	Native	S_TP_CLKOUTFLEX2	20K IN-PD	---	NU
GPIO[67]	CLKOUTFLEX3/GPIO67	AU8	I/O	Core	Native	C_14M_TPM_R	20K IN-PD	---	Native
GPIO[68]	TACH4/GPIO68	AT30	I/O	Core	GPI	S_GPI_BRD_REV2	20K IN-PU (only on TACH4)	10k pull-up to +3V (dummy) 220 pull-down to GND	I
GPIO[69]	TACH5/GPIO69	AV35	I/O	Core	GPI	S_USB_HDR_DET#	20K IN-PU (only on TACH5)	8.2k pull-up to +3V	I
GPIO[70]	TACH6/GPIO70	AK28	I/O	Core	Native	S_GPIO70	20K IN-PU (only on TACH6)	10k pull-up to +3V 10k pull-down to GND (dummy)	Strapping
GPIO[71]	TACH7/GPIO71	AT34	I/O	Core	Native	S_GPIO71	20K IN-PU (only on TACH7)	10k pull-up to +3V 10k pull-down to GND (dummy)	Strapping
GPIO[72]	GPIO72	AJ40	I/O	Suspend	Native (Mobile Only)	S_GPIO72		10k pull-up to +3V_S5	NU
GPIO[73]	PCIECLKRQ0#/GPIO73	W34	I/O	Suspend	Native	S_FP_CHAS_DET#		10k pull-up to +3V_S5	NU
GPIO[74]	SML1ALERT#/TEMP_ALERT#/GPIO74 PCHHOT#	AJ39	I/O	Suspend	Native	TMIN_SHIFT	--	8.2k pull-up to +3V_S5 330k pull-down to GND (Dummy)	O
GPIO[75]	SML1DATA/GP75	AK33	I/O	Suspend	Native	S_SML1DATA	PU	2.2k pull-up to +3V_S5	Native

DELL INC.

Title: GPIO Table

DWG NO: Amazon USFF

Rev: A00

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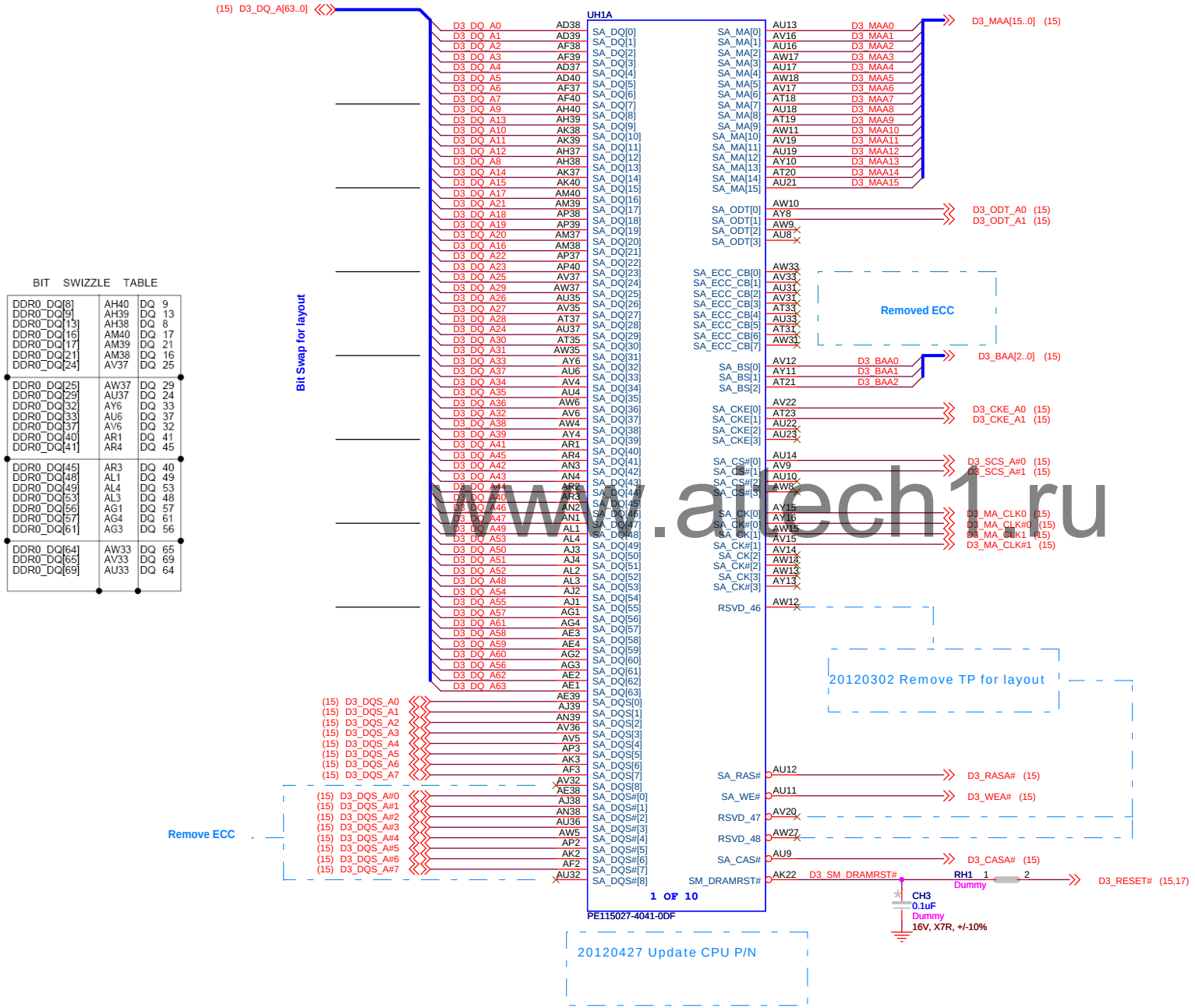
DDR3 CH-A



DELL INC.

Title

CPU-1: DDR3_CHA

DWG NO *Amazon USFF*

Rev A00

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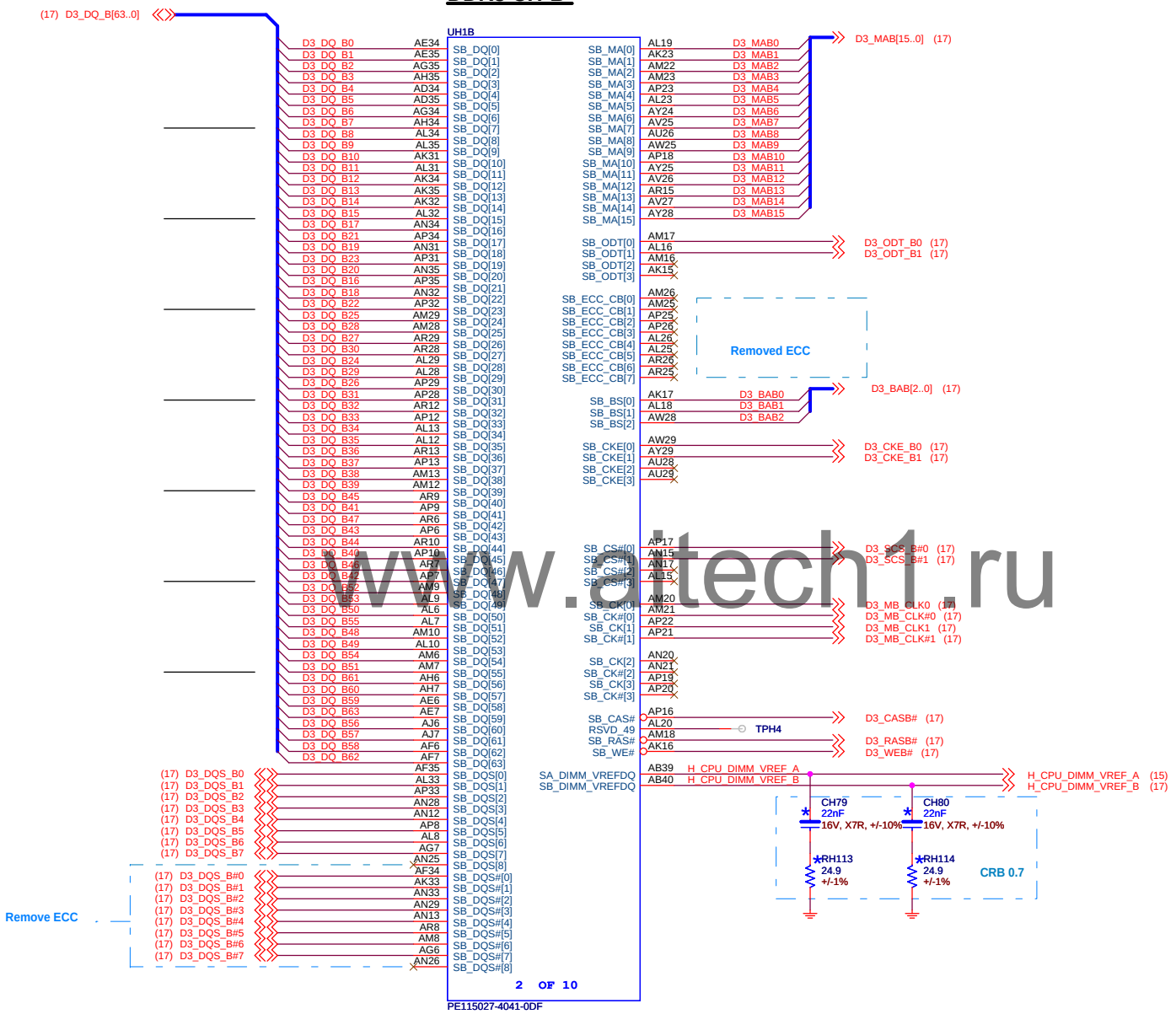
DDR3 CH-B



DELL INC.

Title

CPU-2: DDR3_CHB

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Amazon USFF	A00

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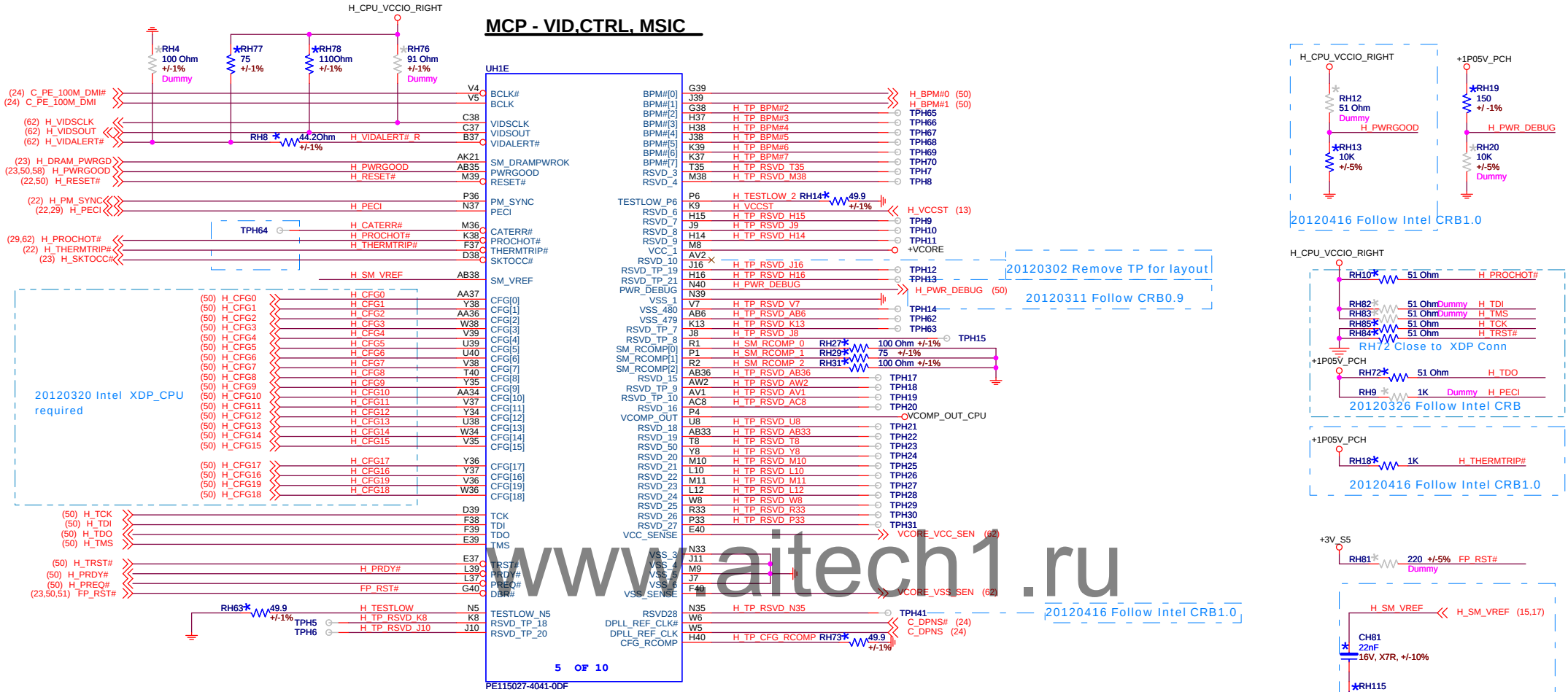
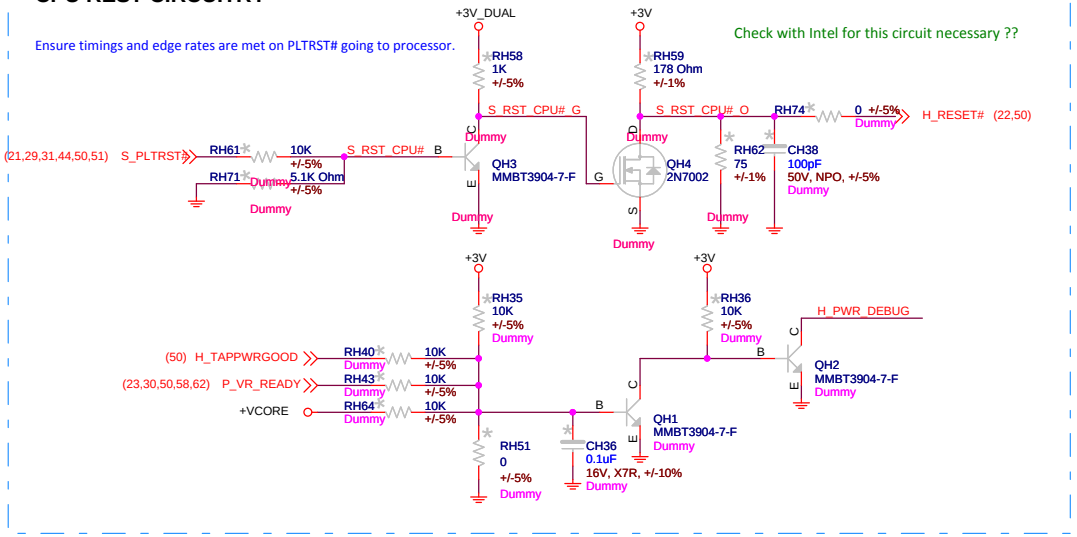
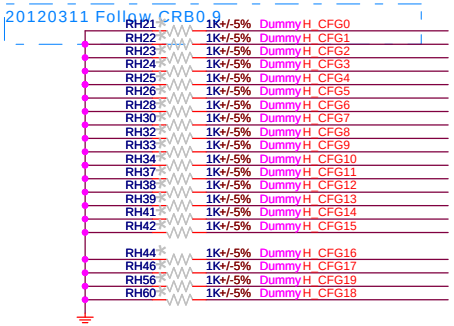
MCP - VID,CTRL, MSIC



CPU REST CIRCUITRY



20120311 Follow CRB0.9



DELL INC.

Title

CPU-3: VID/MISC

DWG NO **Amazon USFF** Rev **A00**

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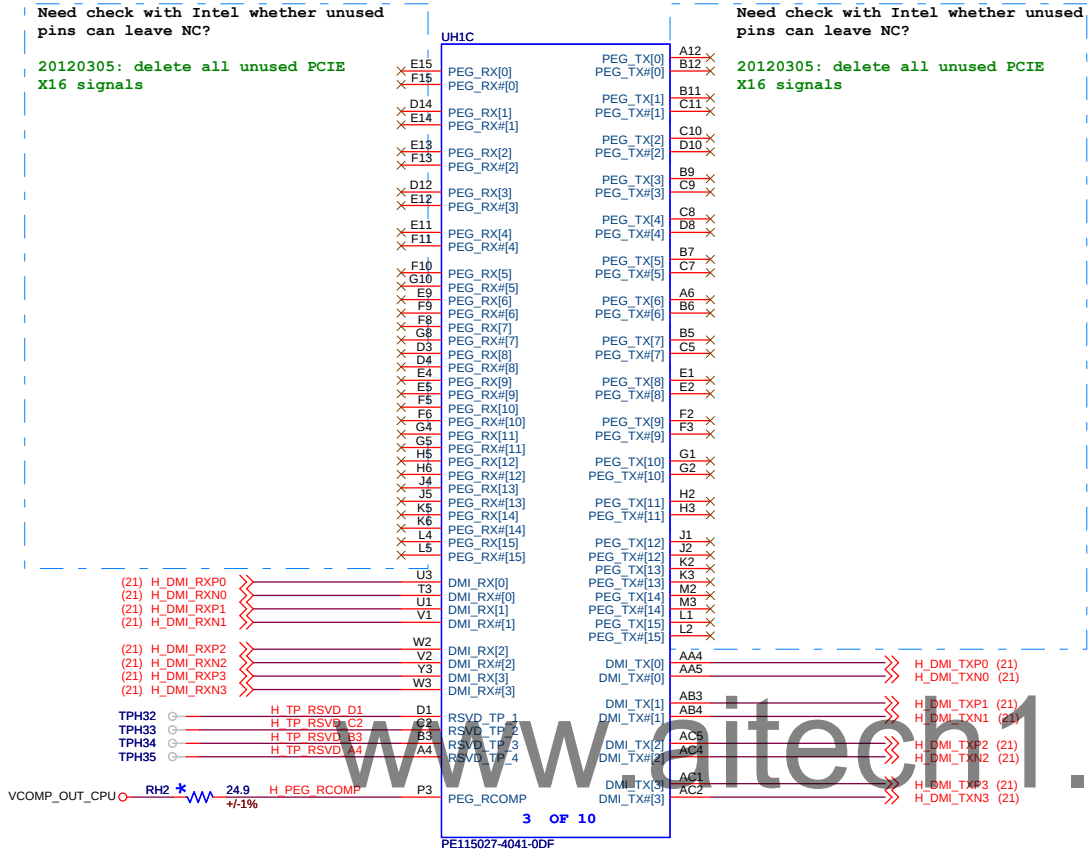
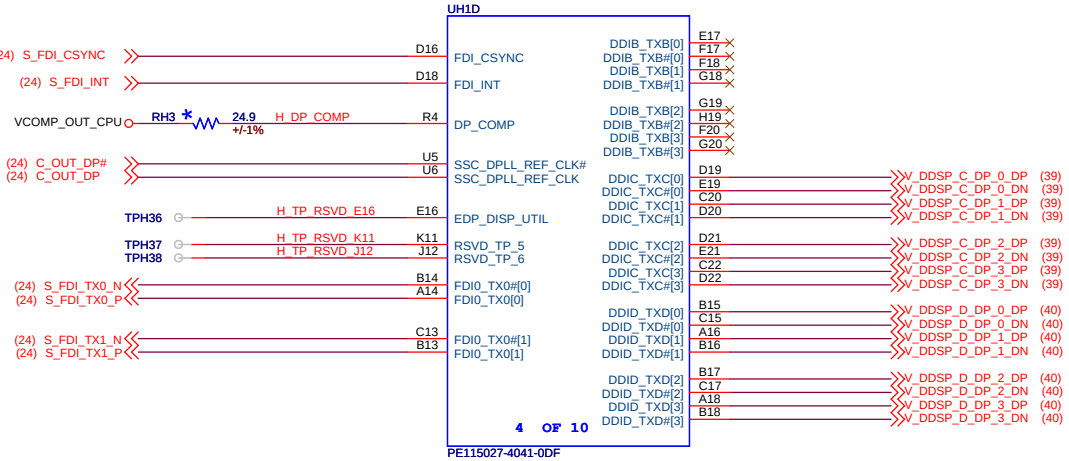
Need check with Intel whether unused pins can leave NC?

20120305: delete all unused PCIE X16 signals



Need check with Intel whether unused pins can leave NC?

20120305: delete all unused PCIE X16 signals



Display Port1

Display Port2

DELL INC.

Title: **CPU-4: FDI/PCIe/DMI/DP**

DWG NO: *Amazon USFF*

Rev: A00

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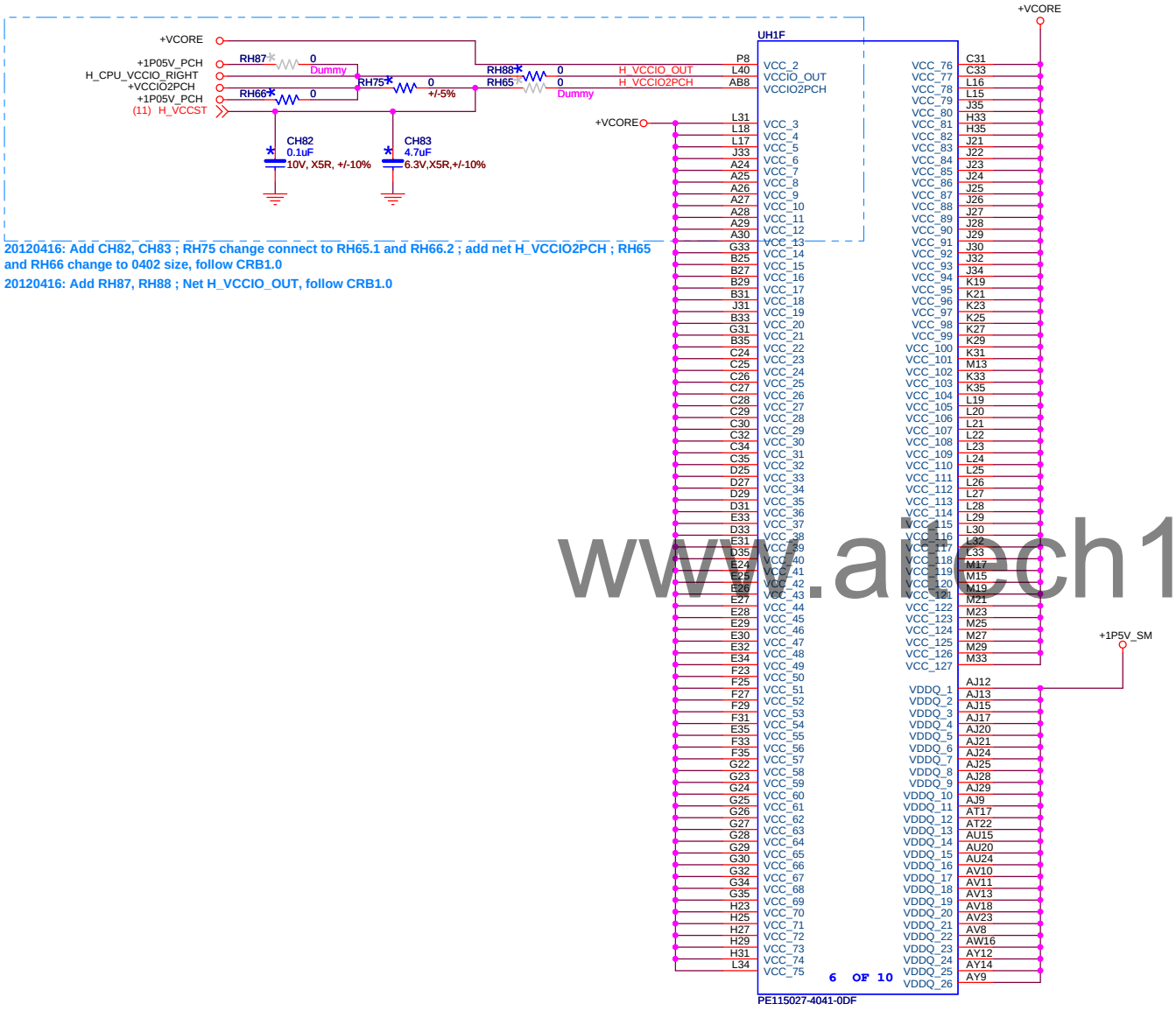

20120416: Add CH82, CH83 ; RH75 change connect to RH65.1 and RH66.2 ; add net H_VCCIO2PCH ; RH65 and RH66 change to 0402 size, follow CRB1.0

20120416: Add RH87, RH88 ; Net H_VCCIO_OUT, follow CRB1.0

DELL INC.

Title

CPU-5: Vcore

DWG NO

Amazon USFF

Rev

A00

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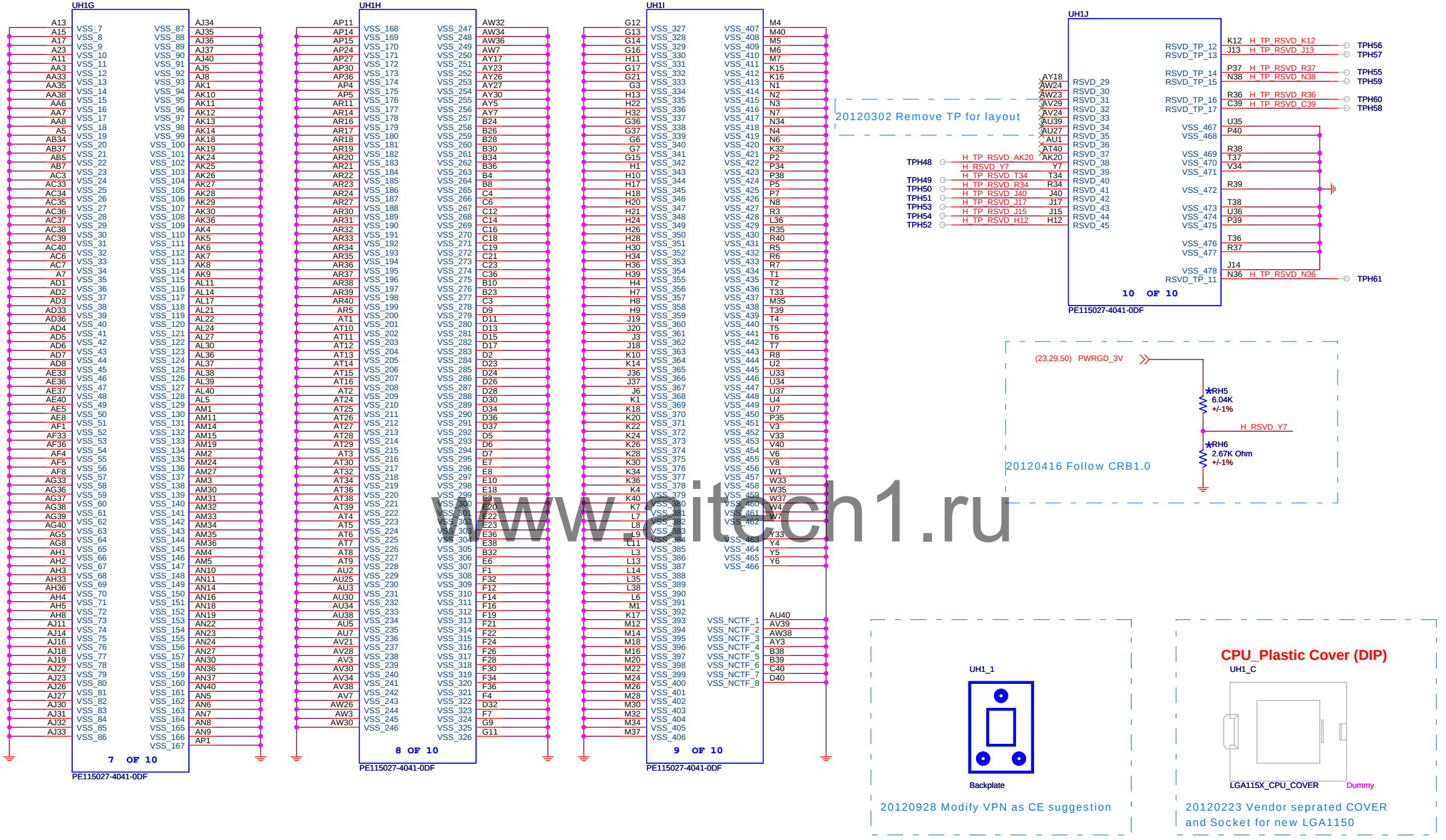

DELL INC.

Title

CPU-6: GND

DWG NO

Amazon USFF

Rev

A00

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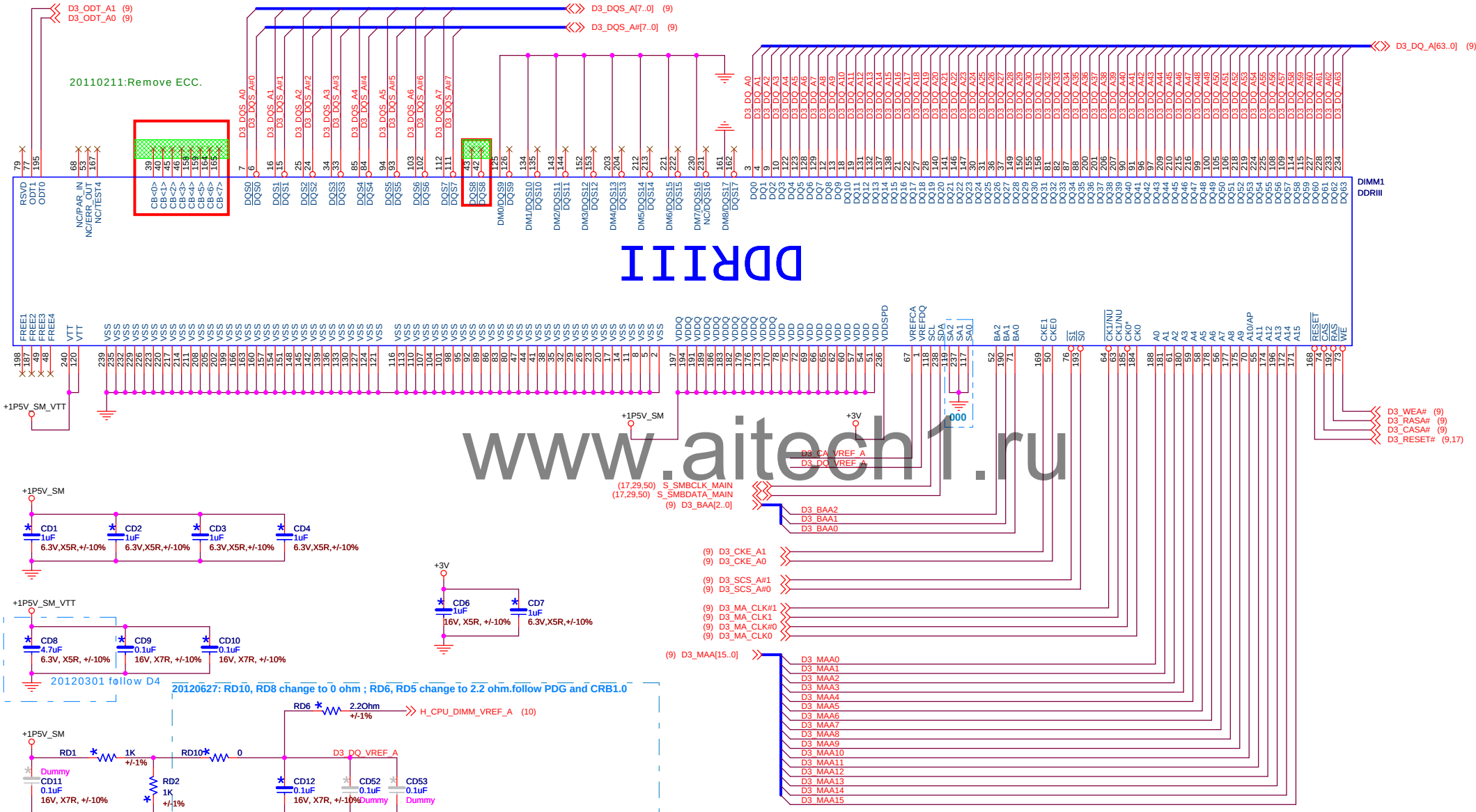
CHANNEL A BANK 1
SMB ADDRESS:000



DELL INC.

Title
DDR3 Conn: CHA_1 (DIMM3)

DWG NO
Amazon USFF

Rev
A00

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CHANNEL A BANK 2
SMB ADDRESS:001

DELL INC.

Title
DDR3 Conn: CHA_2 (TBD)

DWG NO
Amazon USFF

Rev
A00

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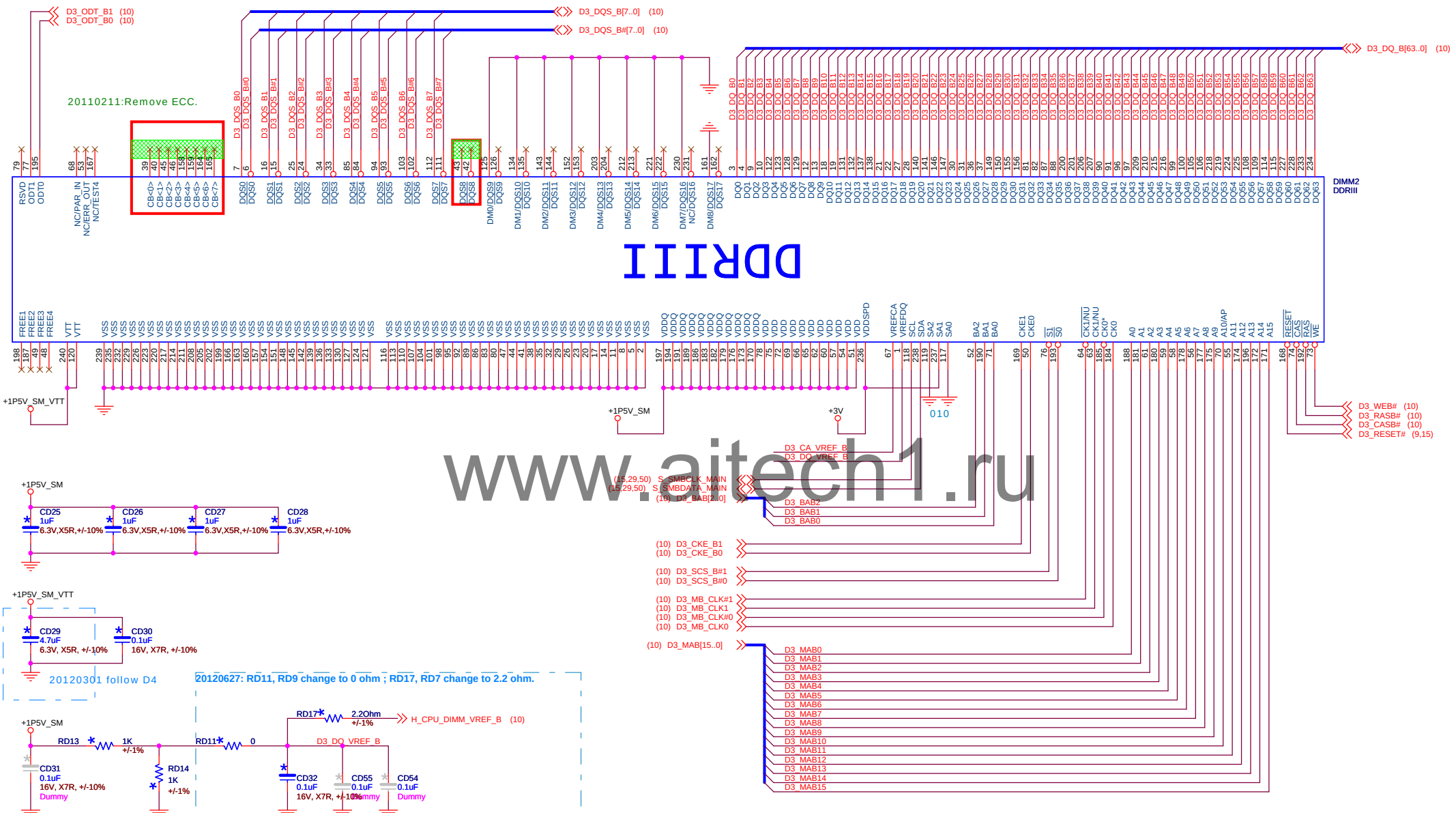
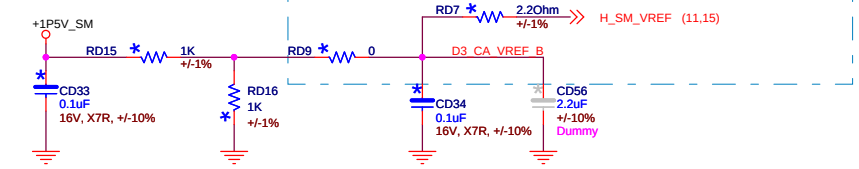
CHANNEL B BANK 1
SMB ADDRESS:010



20120301 follow D4

20120627: RD11, RD9 change to 0 ohm ; RD17, RD7 change to 2.2 ohm.



DELL INC.

Title
DDR3 Conn: CHB_1 (DIMM2)

DWG NO
Amazon USFF

Rev
A00

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DELL INC.

Title

DDR3 Conn: CHB_2 (TBD)

DWG NO

Amazon USFF

Rev

A00

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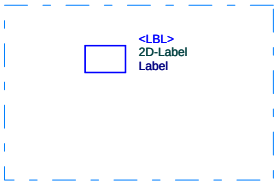

20120322 follow D4 change module fron EMI to Label

DELL INC.

Title

LABEL

DWG NO

Amazon USFF

Rev

A00

Date: Tuesday, January 29, 2013 Sheet 19 of 65

DELL INC.

Title

TBD

DWG NO

Amazon USFF

Rev

A00

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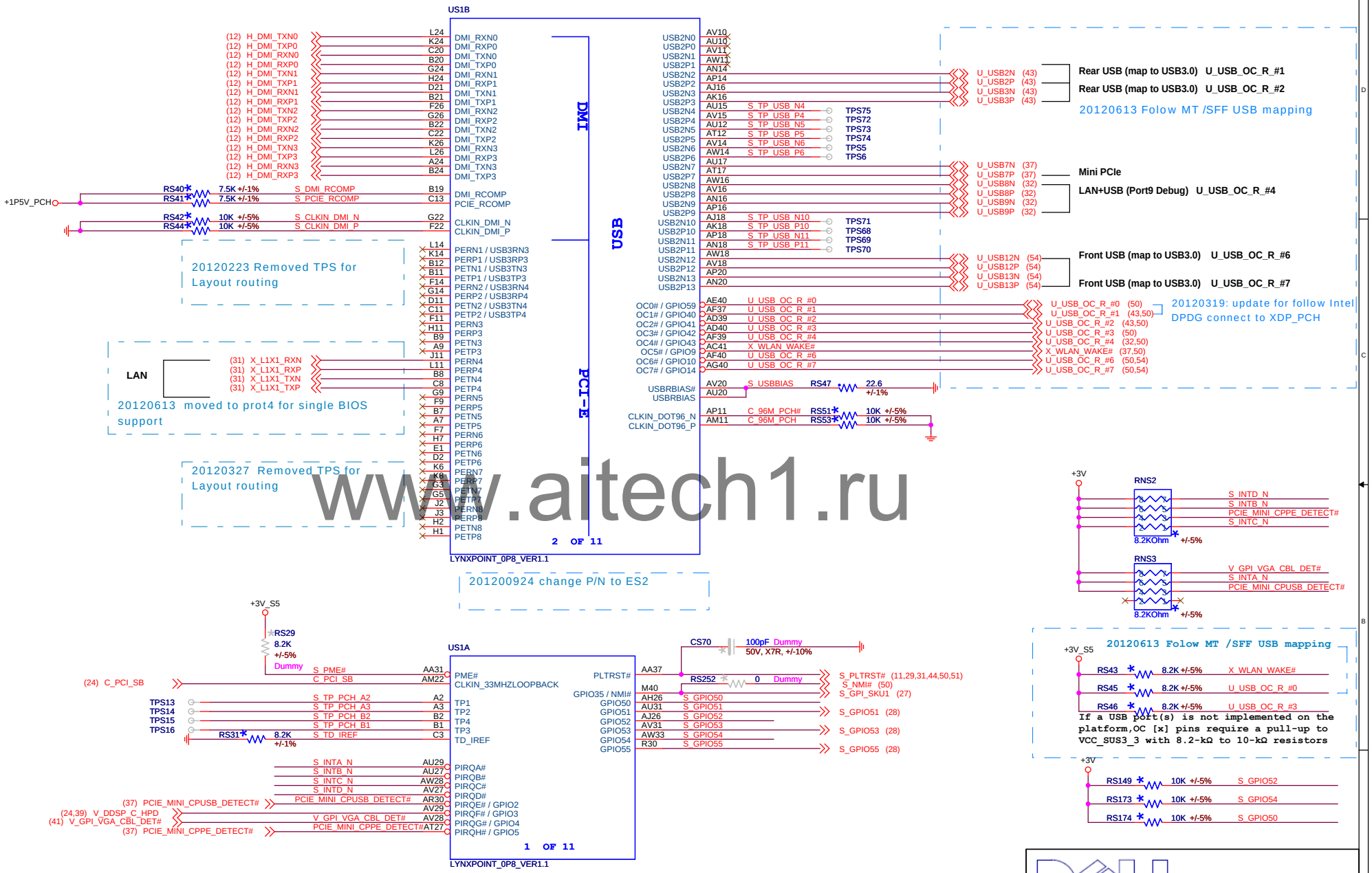

DELL INC.

Title

PCH-1: DMI/USB/PCIe

DWG NO

Amazon USFF

Rev

A00

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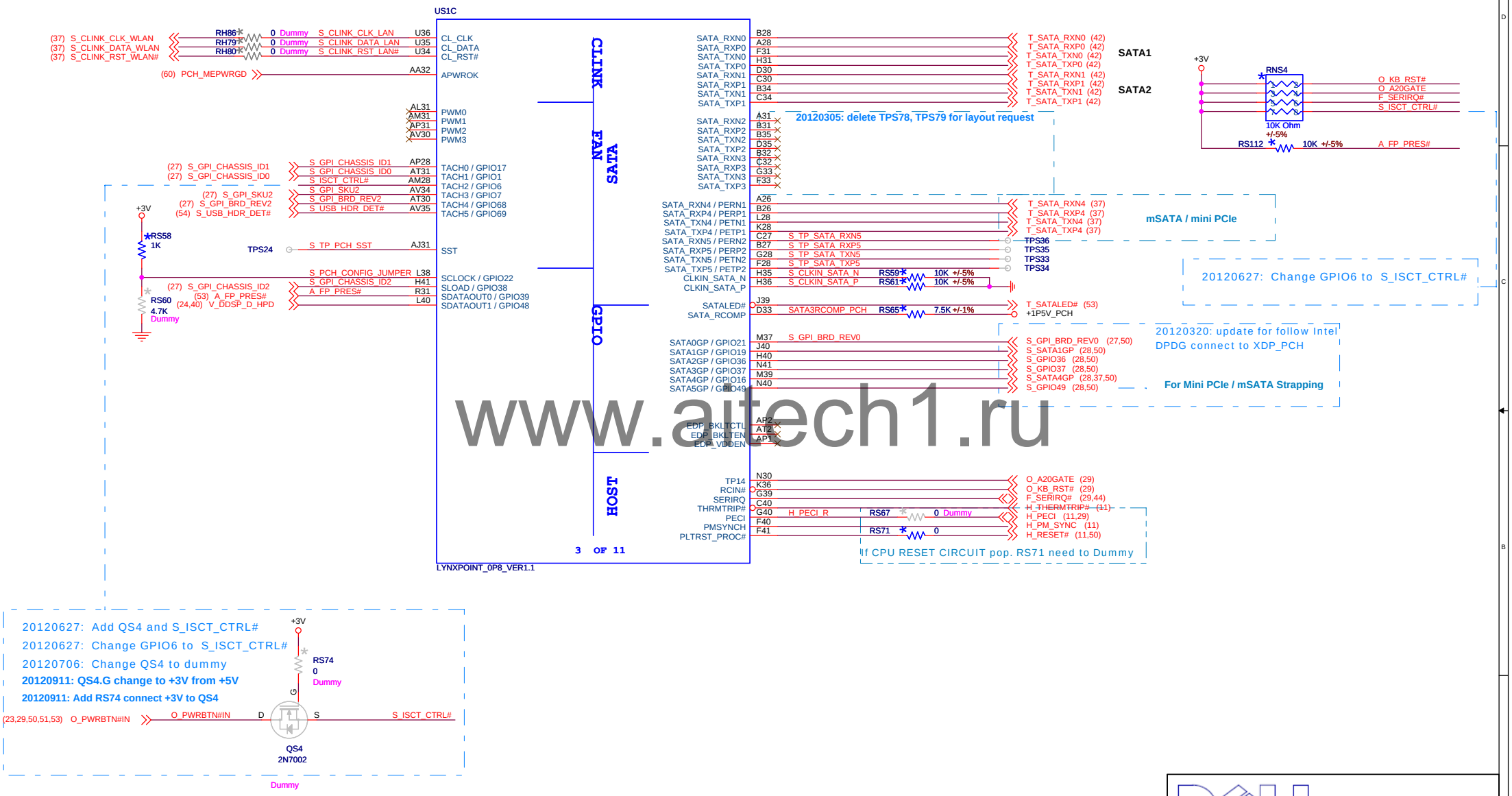

DELL INC.

Title: **PCH-2: SATA/HOST/GPIO**

DWG NO: **Amazon USFF**

Rev: **A00**

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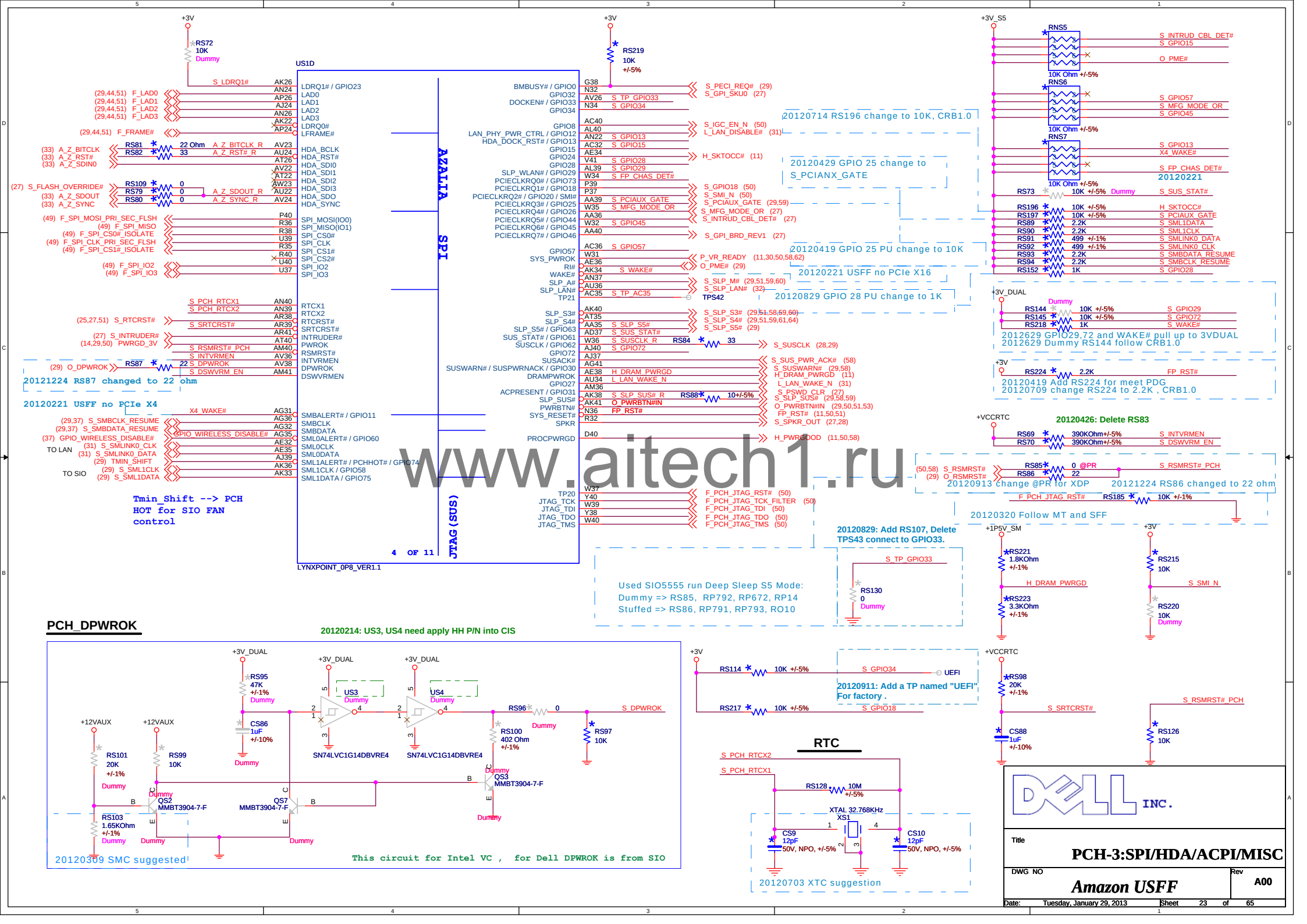
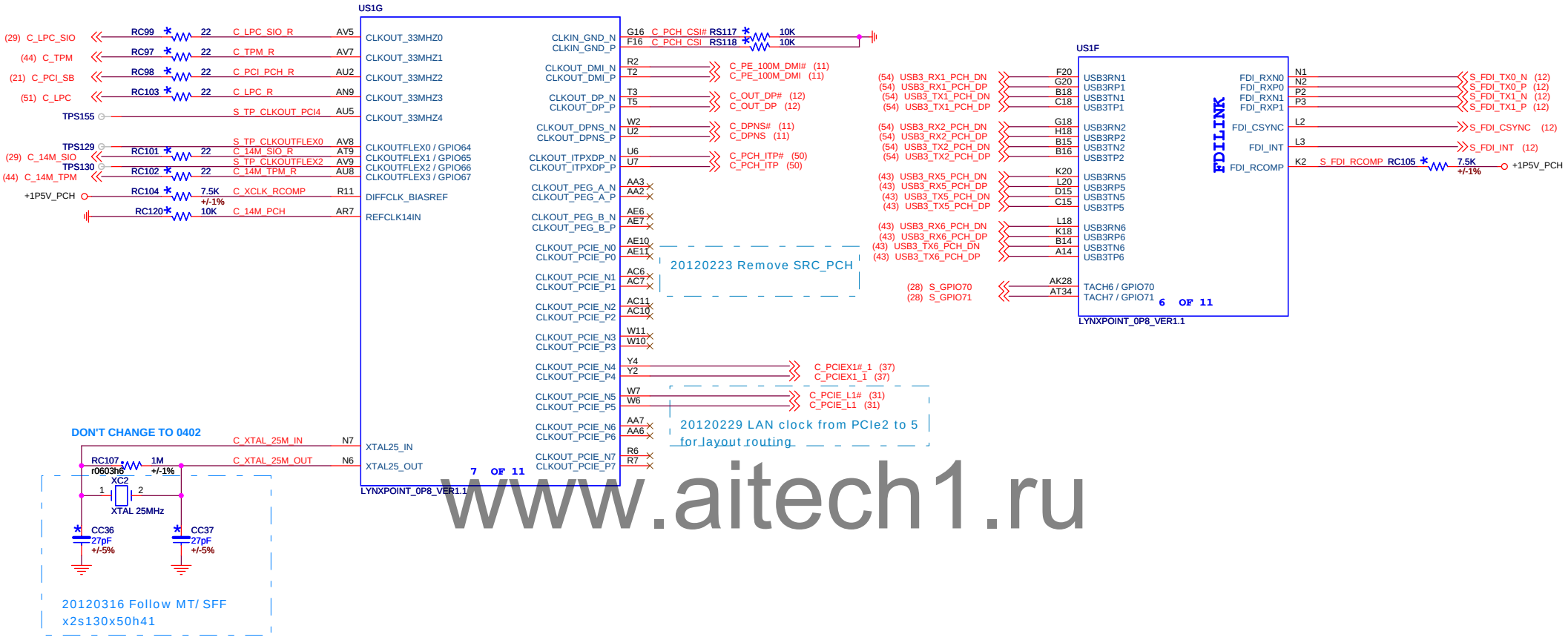
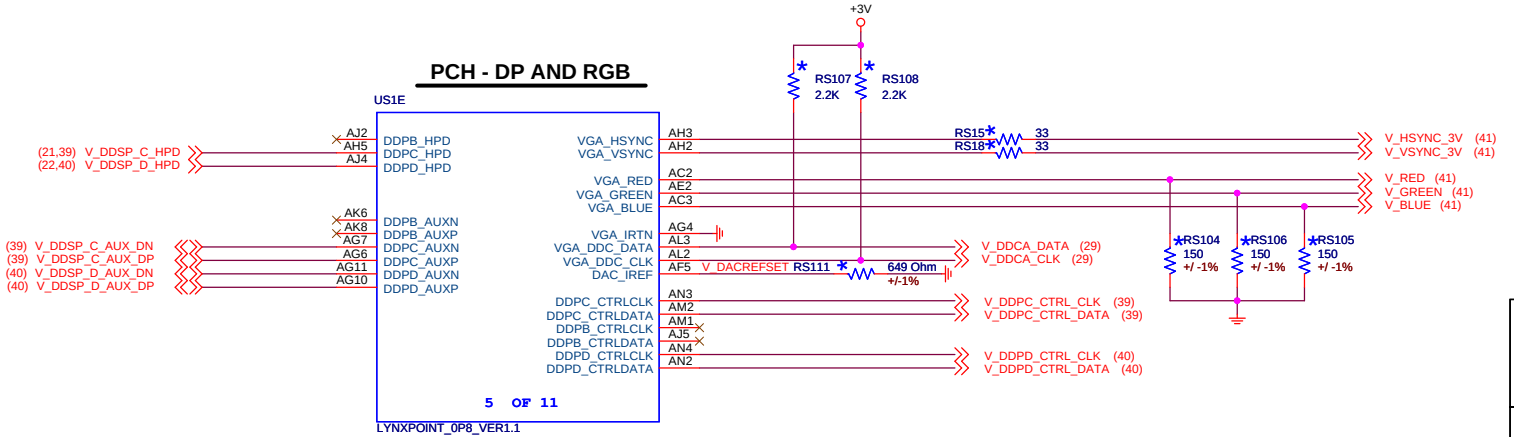


PCH - CLOCK DISTRIBUTION



PCH - DP AND RGB



DELL INC.

Title

PCH-4: VGA/USB3/CLK/FDI

DWG NO	Rev
Amazon USFF	A00

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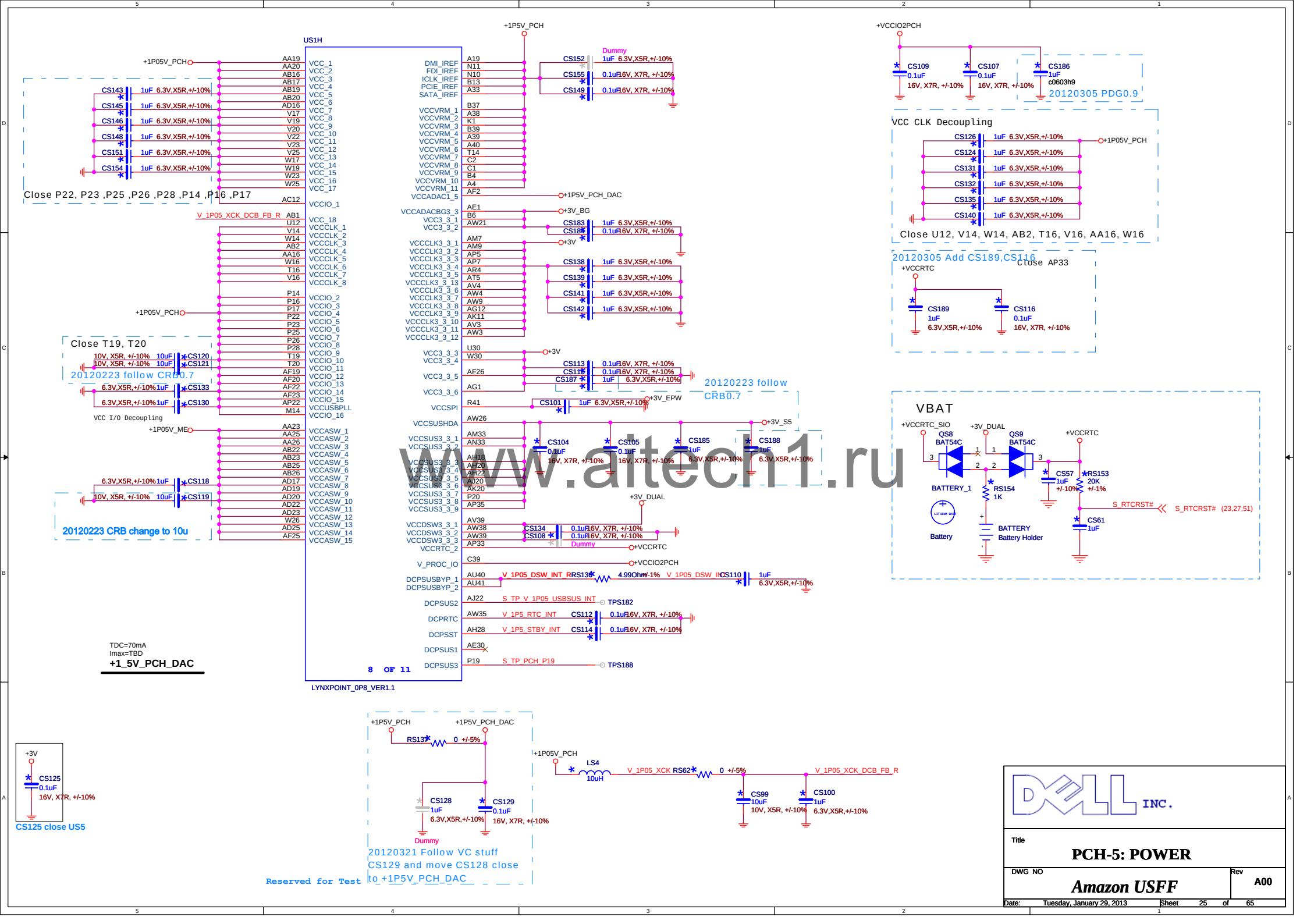

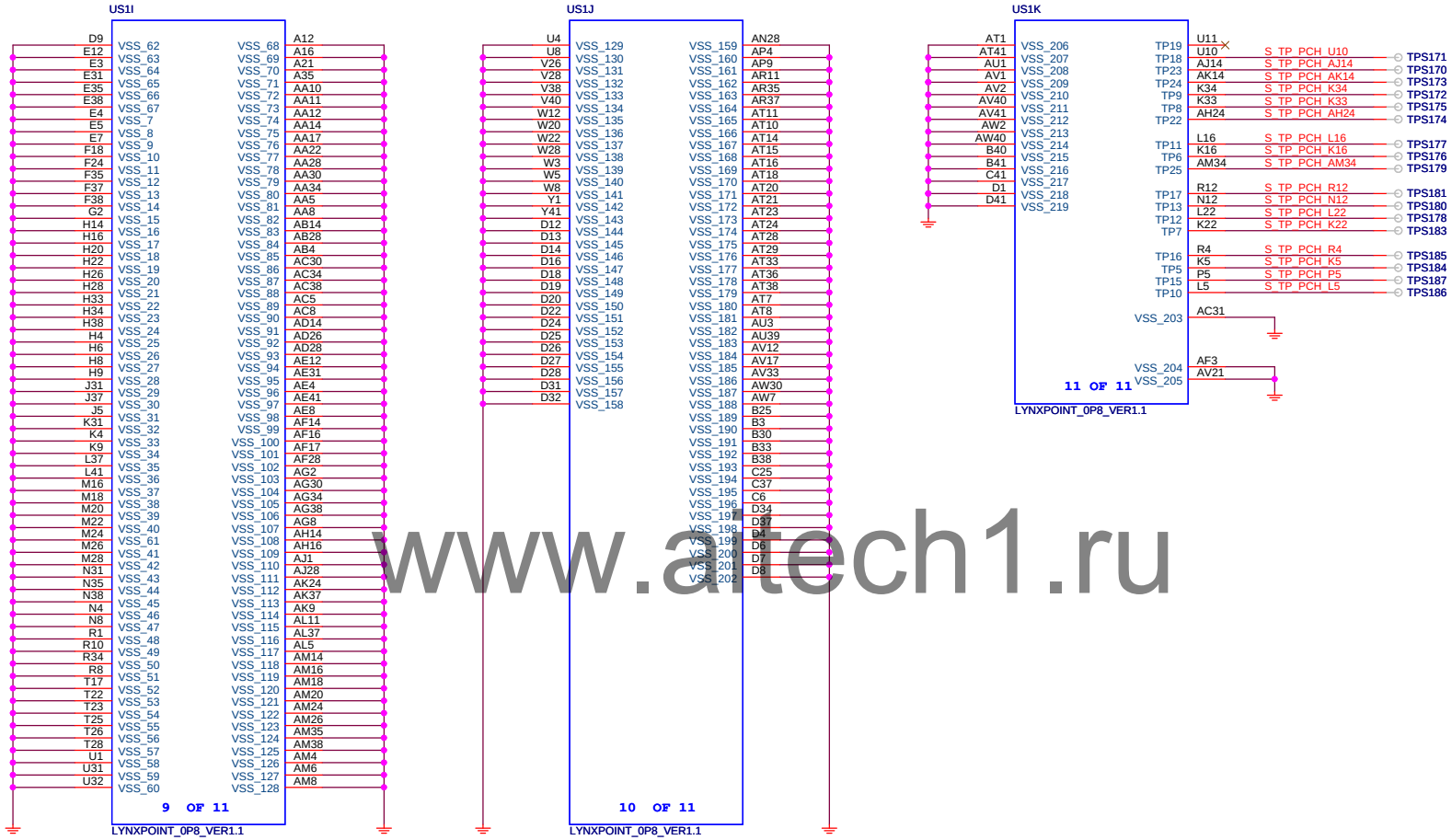

DELL INC.

Title

PCH-6: GND

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Rev

A00

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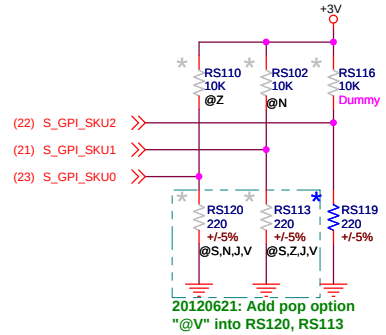
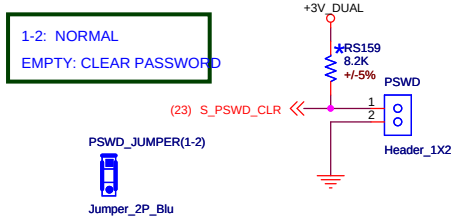
SKU ID

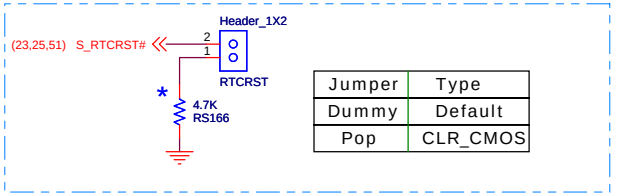


SKU1	SKU0	Type
0	0	TPM
0	1	TCM
1	0	NO TPM/NO TCM
1	1	Reserved

Clear Password

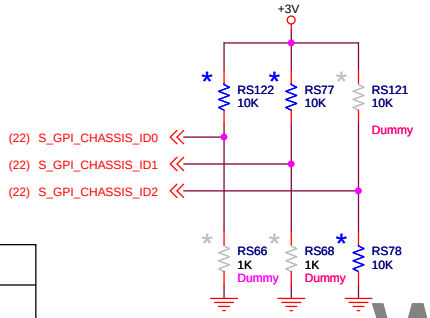


CLR_CMOS



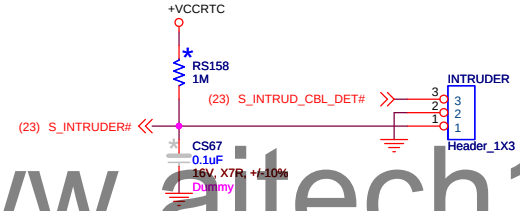
Jumper	Type
Dummy	Default
Pop	CLR_CMOS

Chassis ID

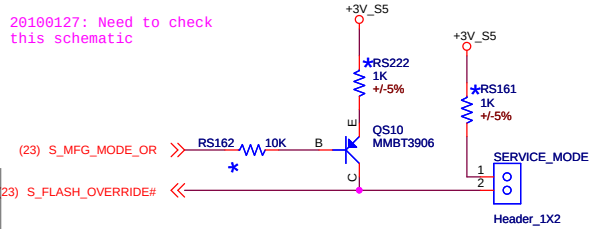


ID2	ID1	ID0	Type
1	0	1	SFF
1	0	0	Reserved
0	0	0	MT/DT
0	1	1	USFF

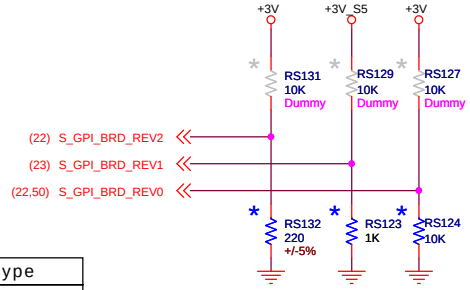
Chassis Intruder



ME Disable (Flash overide)

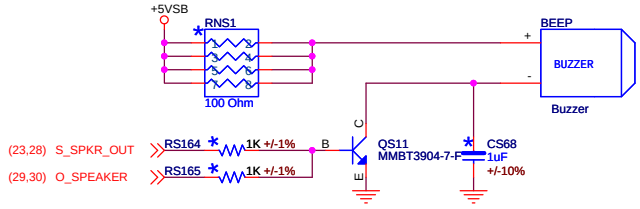


BOARD ID



Rev2	Rev1	Rev0	Type
0	0	0	Default
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

BEEP



PCH HeatSink

20120316 Follow D4
Reomove it

DELL INC.

Title: **PCH-8: MISC CONN/BEEP/ID**

DWG NO: *Amazon USFF* Rev: A00

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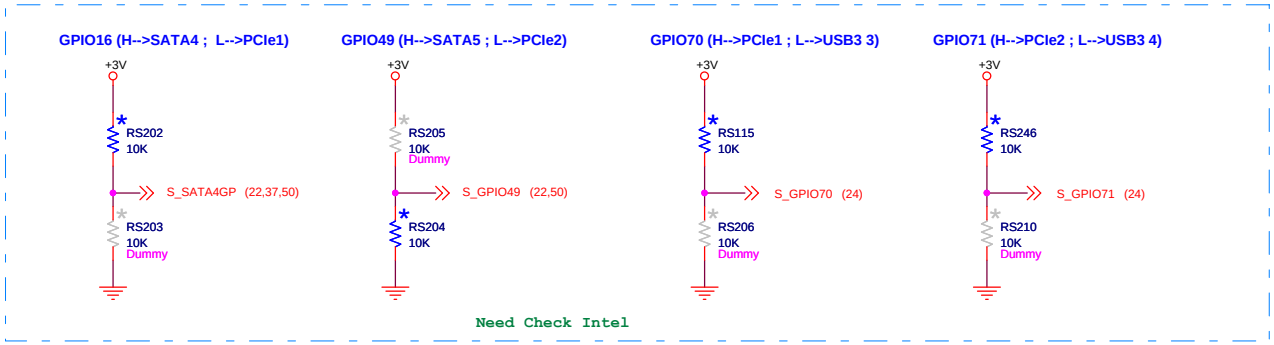
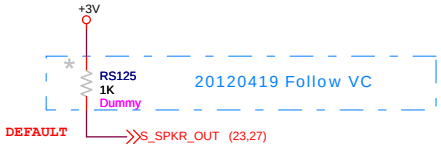


No Reboot Mode

SPKR (IN-PD)	Description
High	No reboot mode: Enable
Low	No reboot mode: Disable



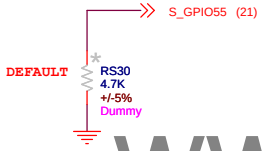
On-Die PLL Voltage Regulator

GPIO62/SUSCLK (IN-PU)	Description
High	Regulator is enabled.
Low	Regulator is disabled.

DEFAULT

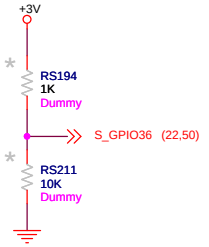
Topblock Swap Mode

GPIO55 (IN-PU)	Description
High	Topblock swap mode: Disable
Low	Topblock swap mode: Enable



DMI Rx Termination

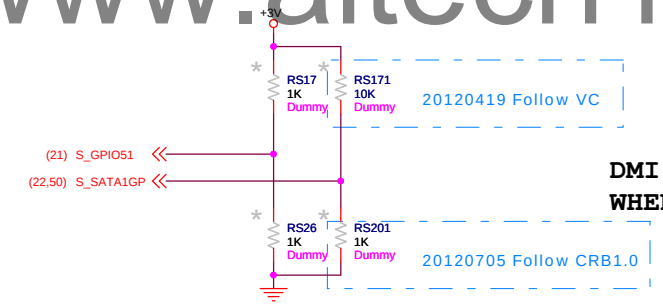
GPIO36 (IN-PD)	Description
Low	DMI Rx Termination Voltage



Boot BIOS Destination Selection

GPIO51 (IN-PU)	SATA1GP/GP19 (IN-PU)	Description
Low	Low	Flash cycle routed to LPC
High	Low	Flash cycle routed to PCI
High	High	Flash cycle routed to SPI

DEFAULT

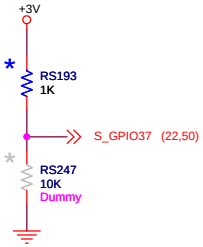


DMI AC COUPLING FULL VOLTAGE MODE WHEN SAMPLED LOW

TLS Confidentiality

GPIO37 (IN-PD)	Description
High	ME Crypto TLS cipher suite with confidentiality
Low	ME Crypto TLS cipher suite with no confidentiality

DEFAULT



DELL INC.

Title: PCH-9: STRAP OPTION

DWG NO: Amazon USFF

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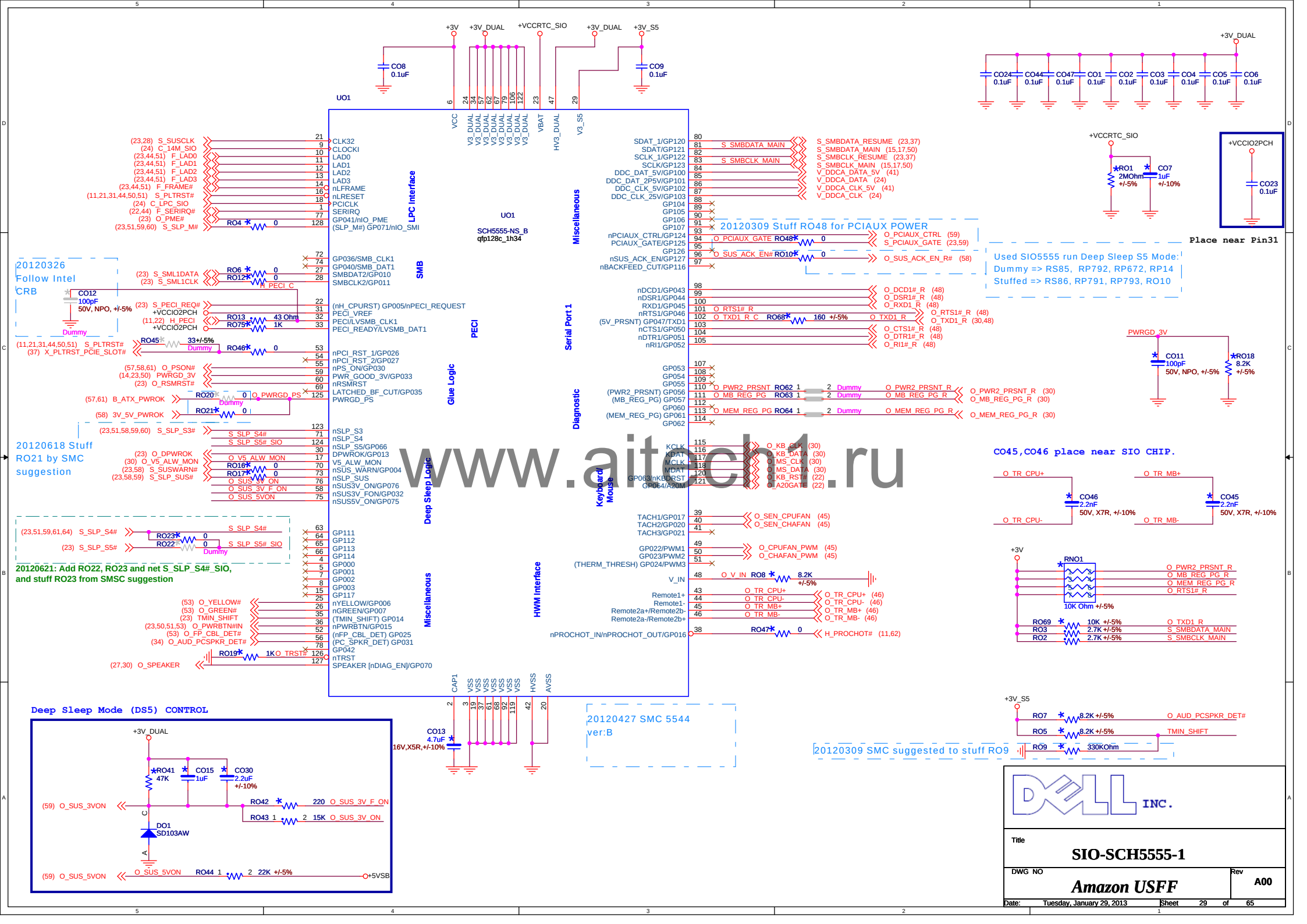
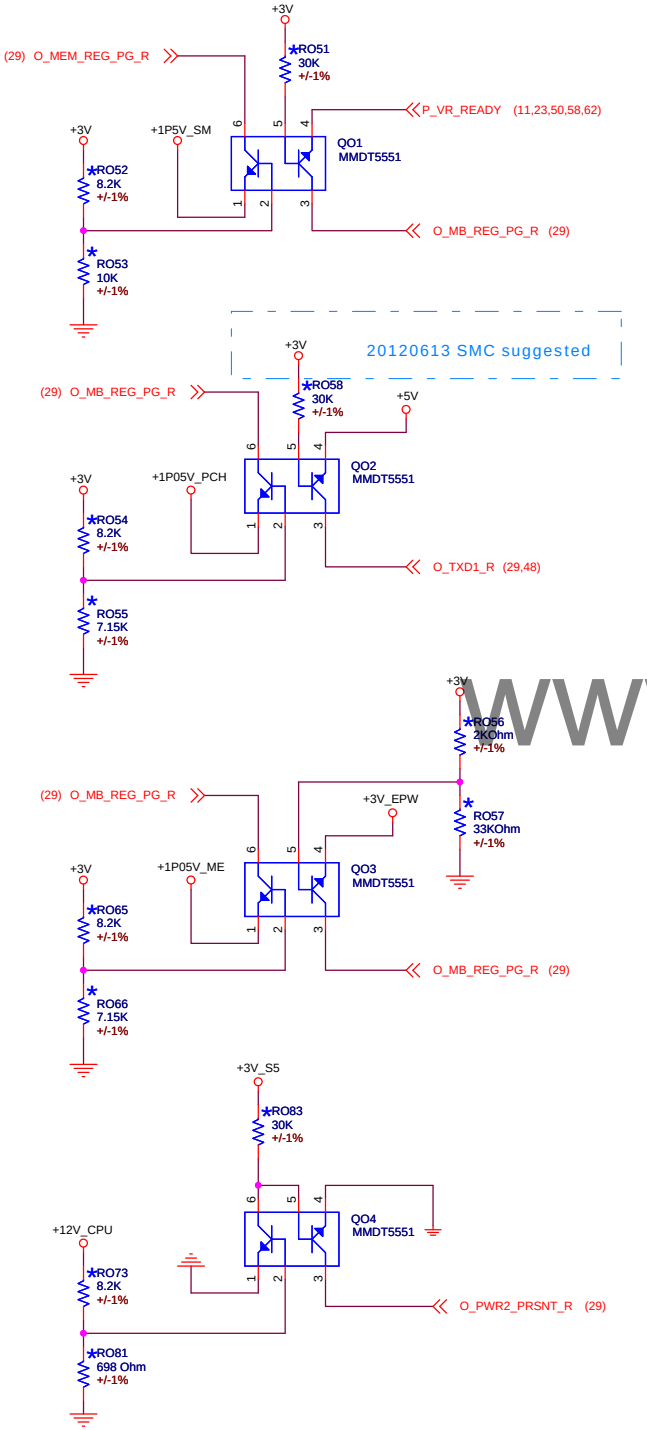
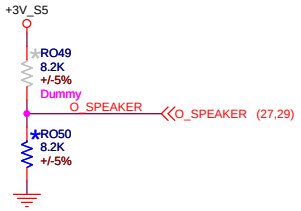


5555 PRE-POST DIAG Monitor



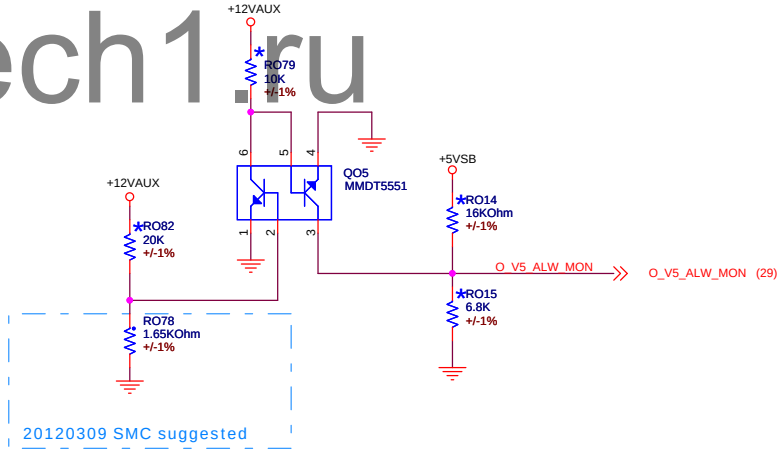
SIO STRAPING

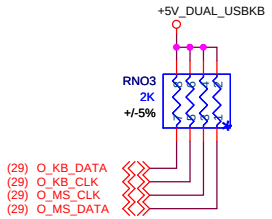


SIO_STRAPING

	SPEAKER	
	Diag_En	
PULL HIGH	Disable	
PULL LOW	Enable	

SIO5555 V5_ALW Monitor





DELL INC.

Title: SIO-SCH5555-2

DWG NO: Amazon USFF

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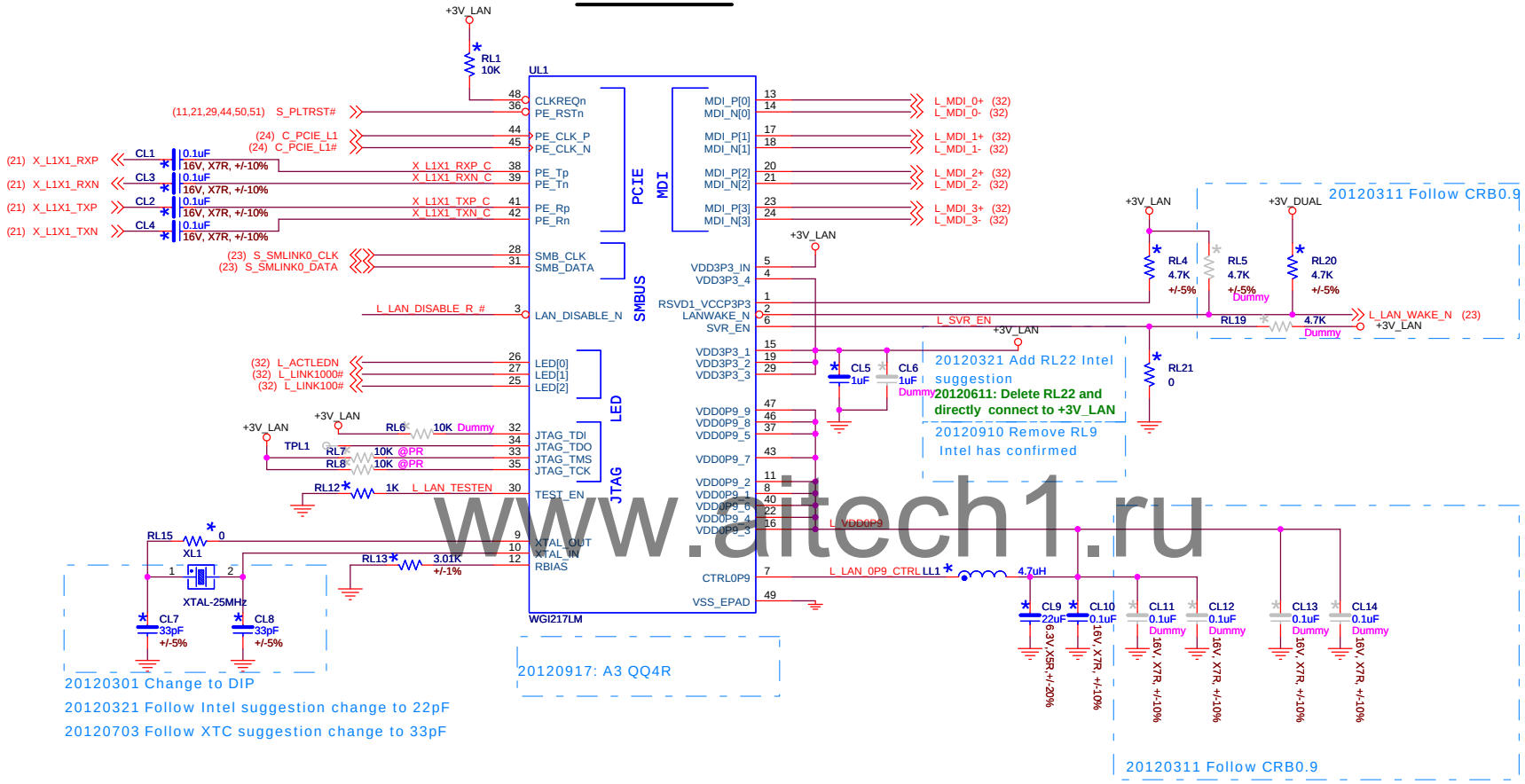
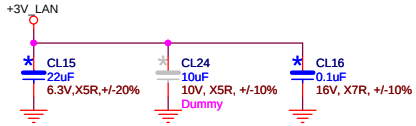
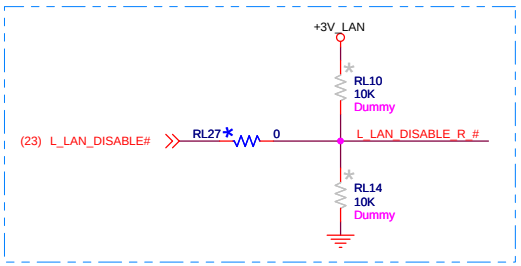
Clarkville need applied CIS.

Intel Clarkville







DELL INC.

Title: **LAN:Intel Clarkville**

DWG NO: ***Amazon USFF***

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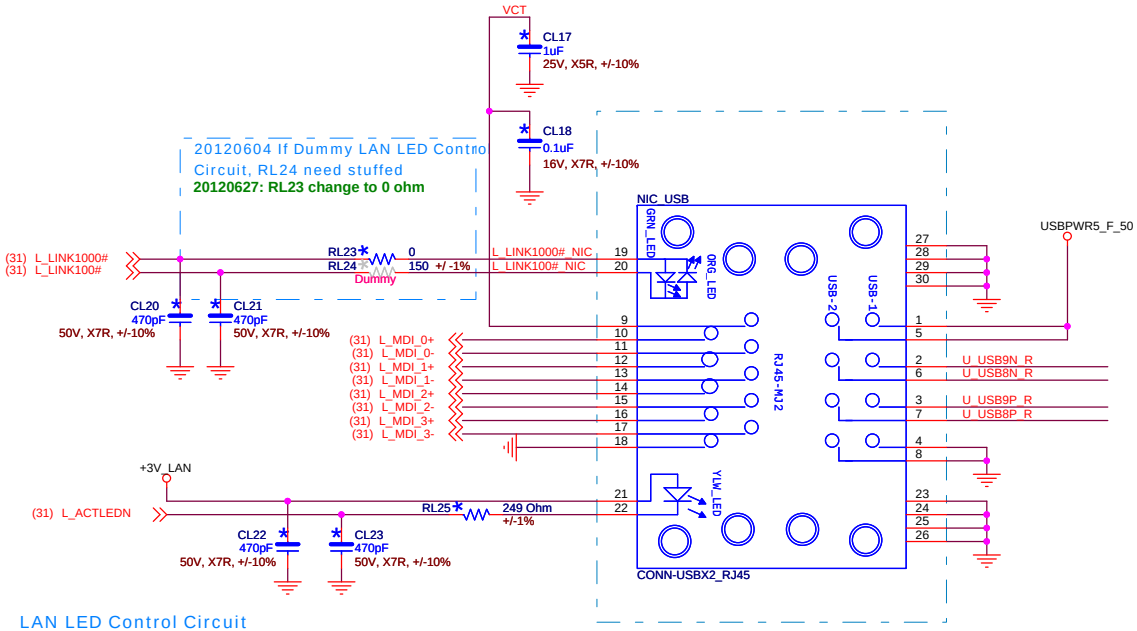
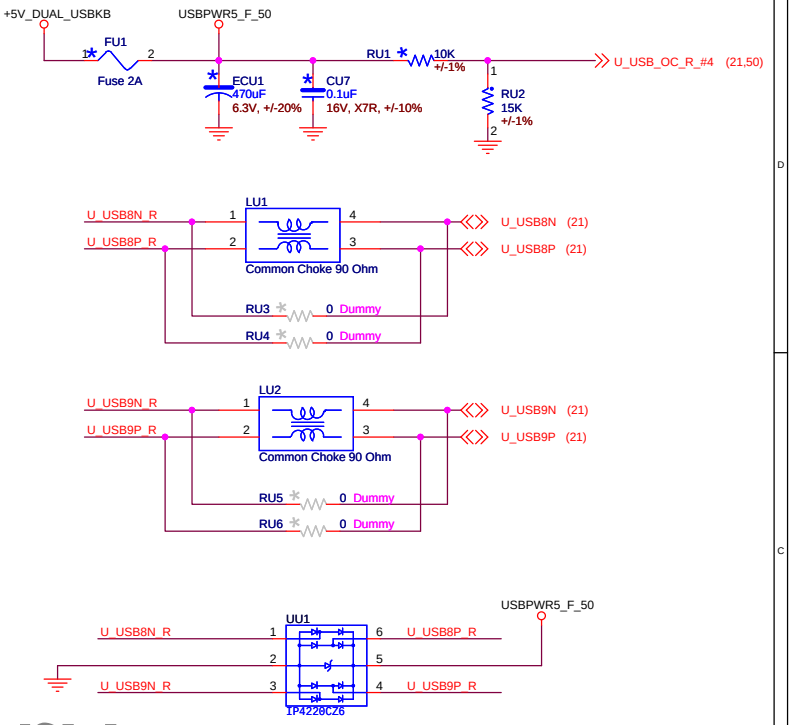
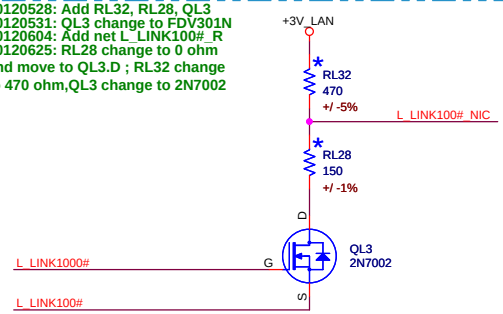
LAN CONNECTOR



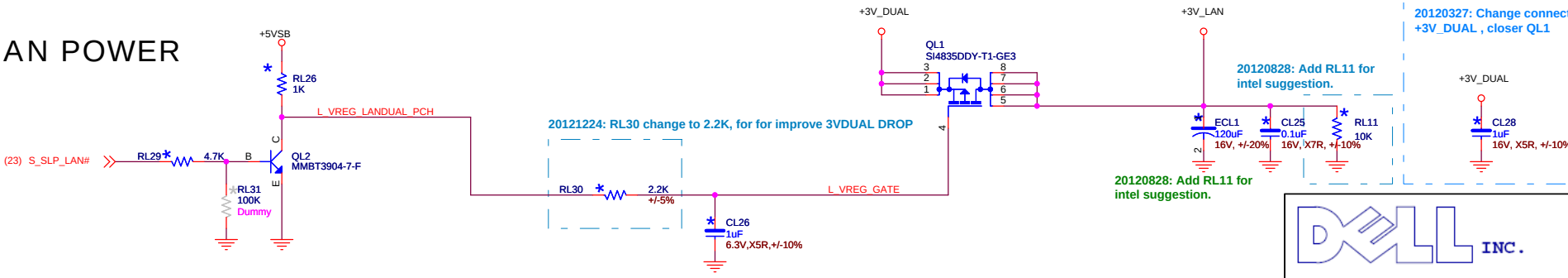


LAN LED Control Circuit

20120528: Add RL32, RL28, QL3
20120531: QL3 change to FDV301N
20120604: Add net L_LINK100#_R
20120625: RL28 change to 0 ohm
and move to QL3.D ; RL32 change
to 470 ohm,QL3 change to 2N7002



LAN POWER



DELL INC.

Title: **LAN Power & LAN/USB Conn**

DWG NO: ***Amazon USFF***

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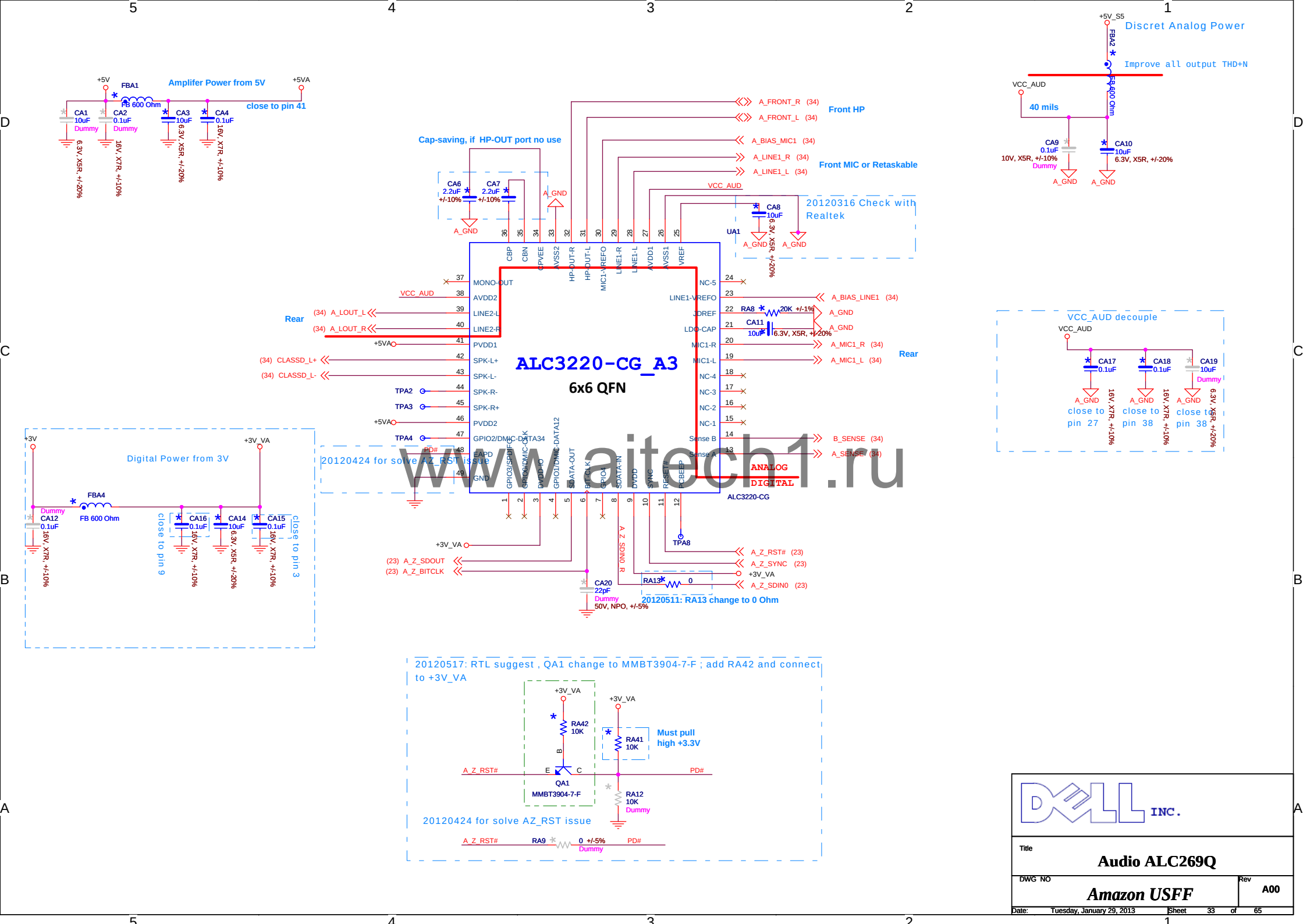

DELL INC.

Title: Audio ALC269Q

DWG NO: Amazon USFF

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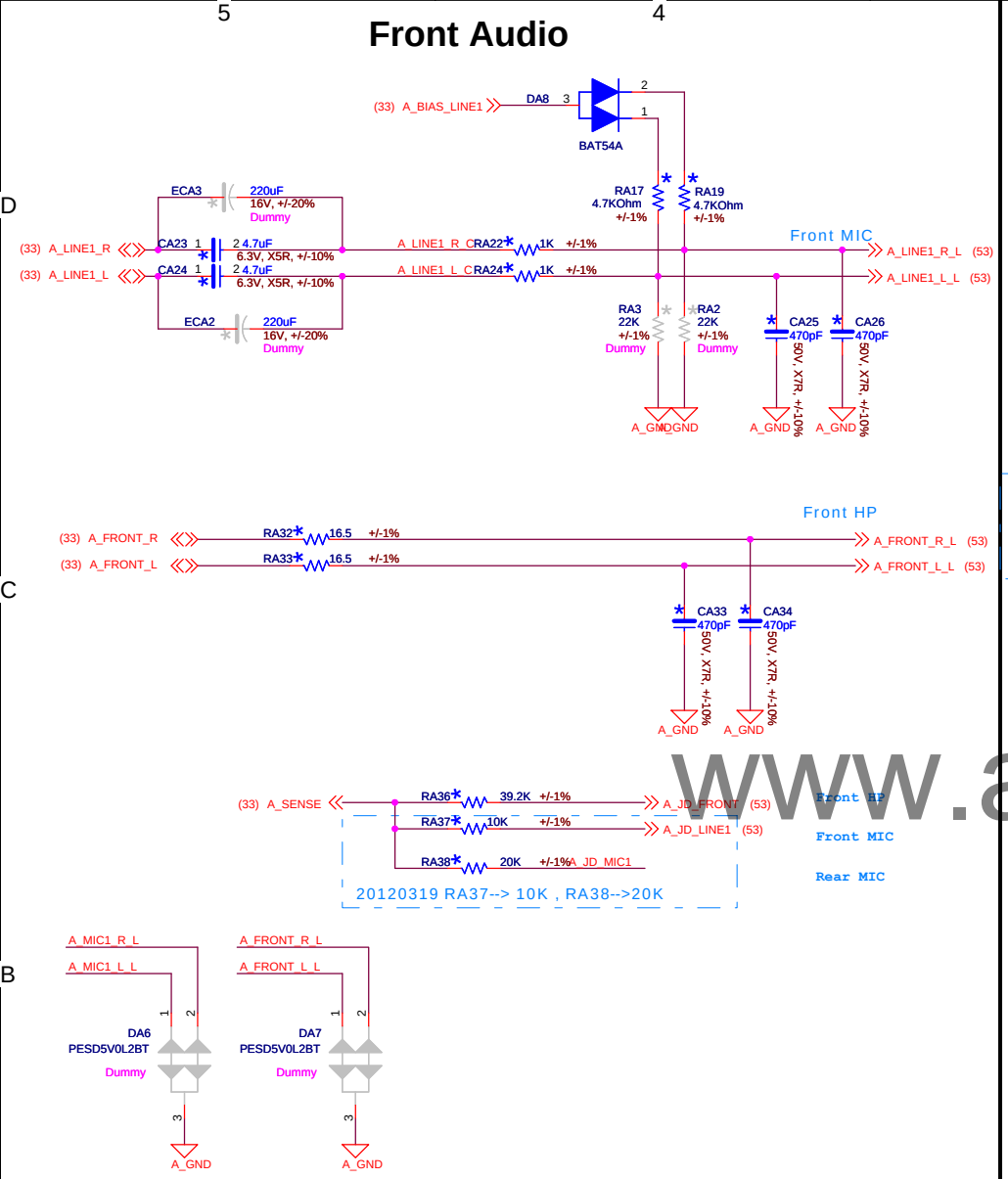
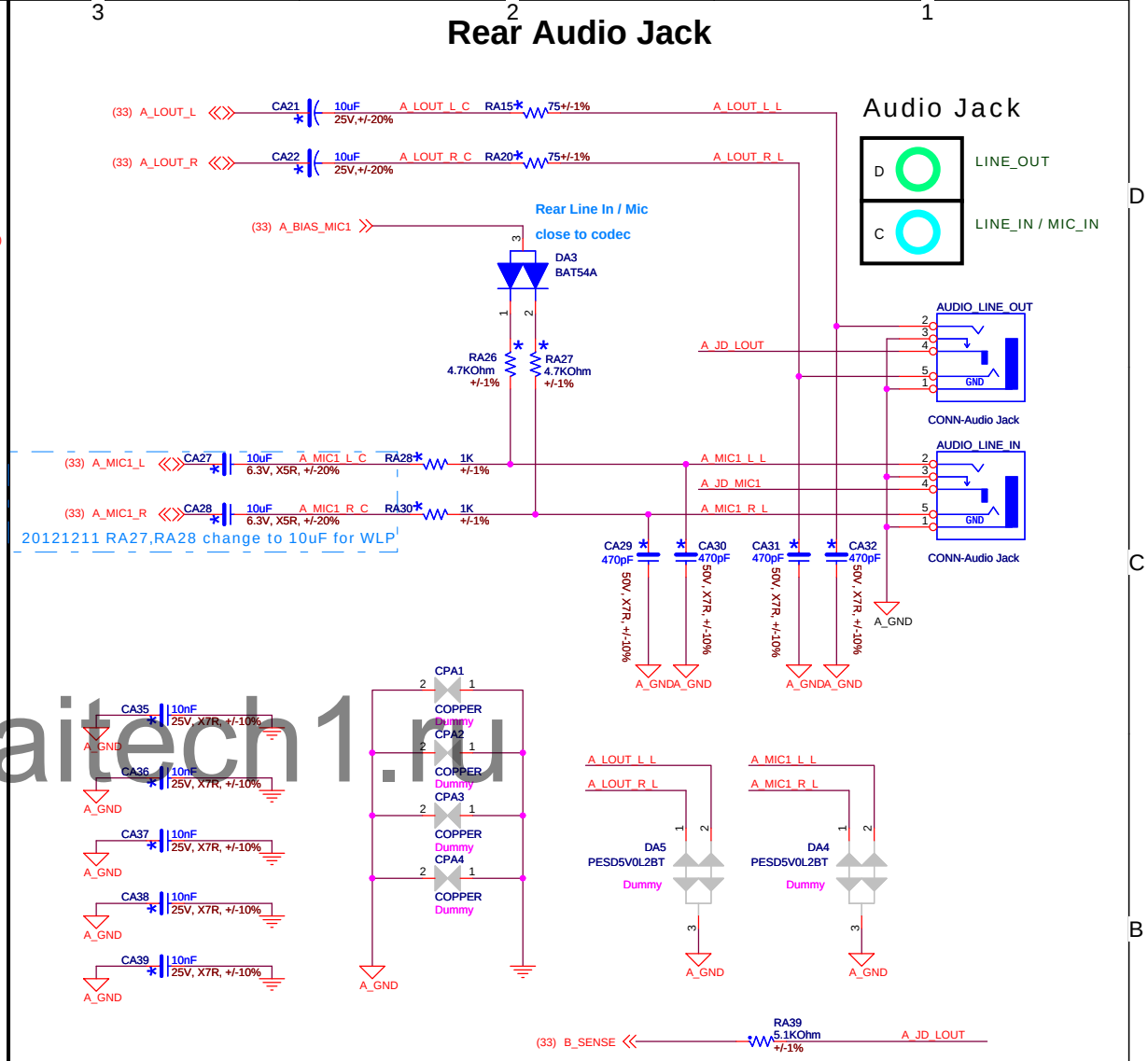
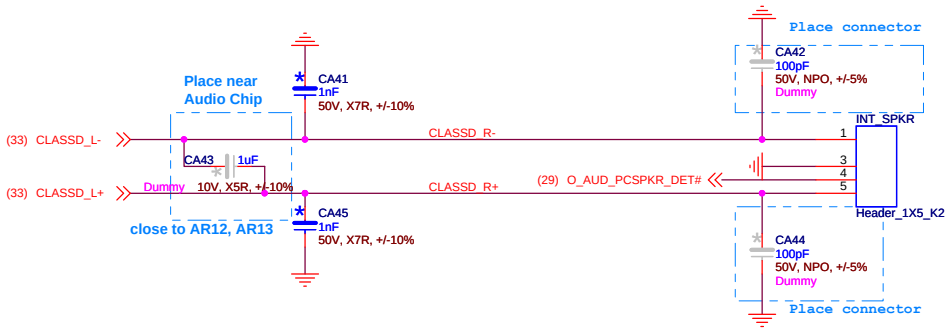
Front Audio



Rear Audio Jack





CHASSIS SPEAKER

Header 1x5 cut2

Pin.1--> Left-
Pin.2--> NC key
Pin.3--> GND
Pin.4--> SPK det#
Pin.5--> Left+

DELL INC.

Title: **Audio Conn**

DWG NO: ***Amazon USFF***

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DELL INC.

Title

Slot1: PCIe 16x (TBD)

DWG NO

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DELL INC.

Title

Slot3: PCIe 1x (TBD)

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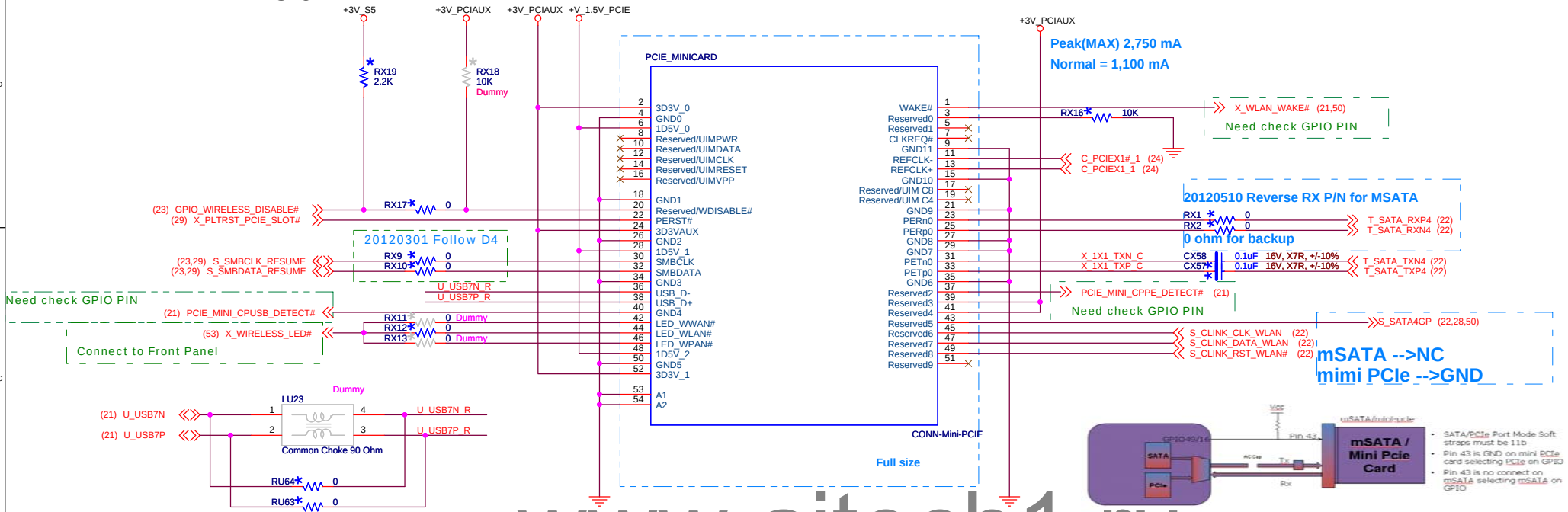
Mini PCIe



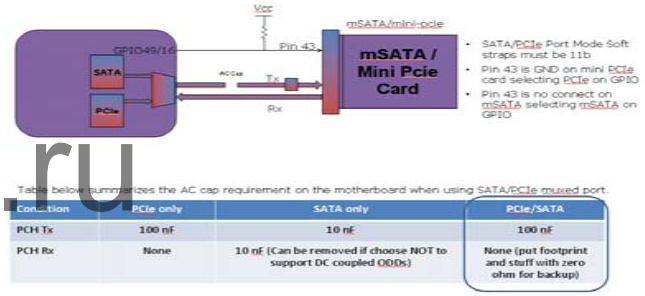
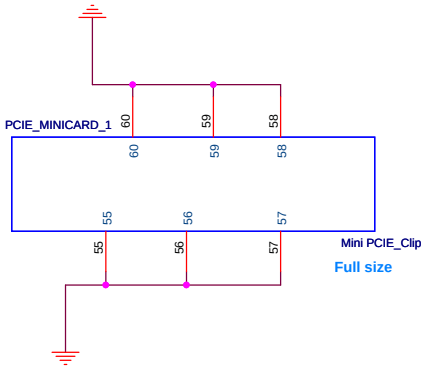


Table below summarizes the AC cap requirement on the motherboard when using SATA/PCIe muxed port.

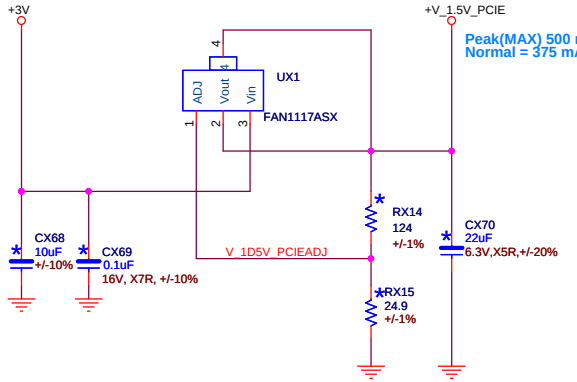
Condition	PCIe only	SATA only	PCIe/SATA
PCH Tx	100 nF	10 nF	100 nF
PCH Rx	None	10 nF (Can be removed if choose NOT to support DC coupled ODDs)	None (put footprint and stuff with zero ohm for backup)

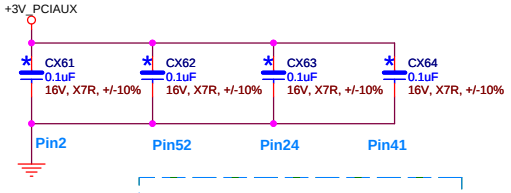
Latch

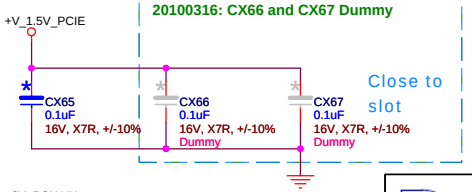


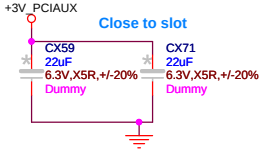
20120320 Dell requested to change Latch

+V_1.5V_PCIE









DELL INC.

Title: **Mini PCIe/MSATA**

DWG NO: **Amazon USFF**

Rev: **A00**

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DELL INC.

Title

Display Port 1

DWG NO

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Rev

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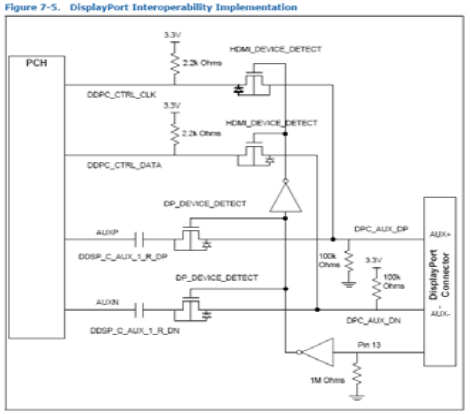
20120521: Delete UV4 ; UV1, UV2, UV3 change to INFINEON_ESD3V3U4ULC

(12) V_DDSP_C_DP_0_DP — CV1 — 0.1uF 16V, X7R, +/-10% — V_DPC_TX0_DP — UV1 pin 9 — pin 1 — V_DPC_TX0_DP
(12) V_DDSP_C_DP_0_DN — CV2 — 0.1uF 16V, X7R, +/-10% — V_DPC_TX0_DN — UV1 pin 8 — pin 2 — V_DPC_TX0_DN
UV1 pin 3 — GND
(12) V_DDSP_C_DP_1_DP — CV3 — 0.1uF 16V, X7R, +/-10% — V_DPC_TX1_DP — UV1 pin 7 — pin 4 — V_DPC_TX1_DP
(12) V_DDSP_C_DP_1_DN — CV4 — 0.1uF 16V, X7R, +/-10% — V_DPC_TX1_DN — UV1 pin 6 — pin 5 — V_DPC_TX1_DN
UV1: ESD3V3U4ULC
Dummy

(12) V_DDSP_C_DP_2_DP — CV5 — 0.1uF 16V, X7R, +/-10% — V_DPC_TX2_DP — UV2 pin 9 — pin 1 — V_DPC_TX2_DP
(12) V_DDSP_C_DP_2_DN — CV6 — 0.1uF 16V, X7R, +/-10% — V_DPC_TX2_DN — UV2 pin 8 — pin 2 — V_DPC_TX2_DN
UV2 pin 3 — GND
(12) V_DDSP_C_DP_3_DP — CV7 — 0.1uF 16V, X7R, +/-10% — V_DPC_TX3_DP — UV2 pin 7 — pin 4 — V_DPC_TX3_DP
(12) V_DDSP_C_DP_3_DN — CV8 — 0.1uF 16V, X7R, +/-10% — V_DPC_TX3_DN — UV2 pin 6 — pin 5 — V_DPC_TX3_DN
UV2: ESD3V3U4ULC
Dummy

V_DPC_AUX_DN — UV3 pin 9 — pin 1 — V_DPC_AUX_DN
V_DPC_AUX_DP — UV3 pin 8 — pin 2 — V_DPC_AUX_DP
UV3 pin 3 — GND
V_DPC_HPD_SINK — UV3 pin 7 — pin 4 — V_DPC_HPD_SINK
DP_P13 — UV3 pin 6 — pin 5 — DP_P13
UV3: ESD3V3U4ULC
Dummy

DP_PORT1
V_DPC_TX0_DP — 1 ML_Lane0_P
2 GND1
V_DPC_TX0_DN — 3 ML_Lane0_N
V_DPC_TX1_DP — 4 ML_Lane1_P
5 GND2
V_DPC_TX1_DN — 6 ML_Lane1_N
V_DPC_TX2_DP — 7 ML_Lane2_P
8 GND3
V_DPC_TX2_DN — 9 ML_Lane2_N
V_DPC_TX3_DP — 10 ML_Lane3_P
11 GND4
V_DPC_TX3_DN — 12 ML_Lane3_N
DP_P13 — 13 GND5
14 GND6
V_DPC_AUX_DP — 15 AUX_CH_P
16 GND7
V_DPC_AUX_DN — 17 AUX_CH_N
V_DPC_HPD_SINK — 18 H_P_DETECT
19 RETURN
V_DPC_PWR — 20 DP_PWR
23 HOLE3 — 22 HOLE2
24 HOLE4 — 21 HOLE1
CONN - Display port
RV1 1M — RV2 100K

Figure 7-5. DisplayPort Interoperability Implementation


20110211:change 2N7002DW for cost down.

QV38: 2N7002DW
V_DDPC_CTRL_CLK — QV38 pin 3
DP_P13_POS — QV38 pin 5
V_DPC_AUX_DP — QV38 pin 6
QV38 pin 4 — QV38 pin 2 — QV38 pin 1
RV3 1M +/-5%

QV37: 2N7002DW
V_DDPC_CTRL_DATA — QV37 pin 3
DP_P13_POS — QV37 pin 5
V_DPC_AUX_DN — QV37 pin 6
QV37 pin 4 — QV37 pin 2 — QV37 pin 1
RV4 1M +/-5%

QV35: 2N7002DW
V_DDSP_C_AUX_DP_C — QV35 pin 3
DP_P13_INV — QV35 pin 5
V_DPC_AUX_DP — QV35 pin 6
QV35 pin 4 — QV35 pin 2 — QV35 pin 1
RV5 1M +/-5%

QV36: 2N7002DW
V_DDSP_C_AUX_DN_C — QV36 pin 3
DP_P13_INV — QV36 pin 5
V_DPC_AUX_DN — QV36 pin 6
QV36 pin 4 — QV36 pin 2 — QV36 pin 1
RV6 1M +/-5%

(24) V_DDSP_C_AUX_DN — CV9 — 0.1uF 16V, X7R, +/-10% — V_DDSP_C_AUX_DN_C
(24) V_DDSP_C_AUX_DP — CV10 — 0.1uF 16V, X7R, +/-10% — V_DDSP_C_AUX_DP_C

+3V — RV7 2.2K +/-5%
+3V — RV8 2.2K +/-5%
(24) V_DDPC_CTRL_CLK — V_DDPC_CTRL_CLK
(24) V_DDPC_CTRL_DATA — V_DDPC_CTRL_DATA

+3V — FV1 FUSE_1.1A — V_DPC_PWR
CV11 1uF 16V,X5R,+/-20%
CV12 10uF Dummy 10V,X5R,+/-20%
CV13 470pF 50V, X7R, +/-10%
CV14 22uF 6.3V,X5R,+/-20%

Display Port Hotplug Detect
+5V — RV15 1K Dummy — V_DPC_HPD_SINK
V_DPC_HPD_SINK — +5V — QV11 FDV301N (D, G, S) — RV19 100K
V_DDSP_C_HPD (21,24)

+3V — RV16 100KOhm +/-1% — V_DPC_AUX_DN
+3V_DUAL — RV17 100KOhm +/-1% Dummy — V_DPC_AUX_DP
+3V — RV18 100KOhm +/-1% Dummy
RV20 100KOhm +/-1% Dummy
RV21 100KOhm +/-1%

+5V — RV12 1K Dummy — DP_P13
RV13 8.2K +/-5%
RV14 1M +/-5%
CV15 0.1uF 16V, X7R, +/-10%

+12V — RV9 4.7K +/-5%
20110211:change 2N7002DW for cost down.
20120312: delete RV11.
DP_P13_INV — QV32 2N7002DW
+12V — RV10 8.2K +/-5% — DP_P13_POS

DELL INC.

Title: Display Port 1
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20120521: Delete UV8 ; UV7, UV9, UV10 change to INFINEON_ESD3V3U4ULC

(12) V_DDSP_D_DP_0_DP — CV43 0.1uF 16V, X7R, +/-10% — V_DPD_TX0_DP
(12) V_DDSP_D_DP_0_DN — CV37 0.1uF 16V, X7R, +/-10% — V_DPD_TX0_DN
(12) V_DDSP_D_DP_1_DP — CV42 0.1uF 16V, X7R, +/-10% — V_DPD_TX1_DP
(12) V_DDSP_D_DP_1_DN — CV45 0.1uF 16V, X7R, +/-10% — V_DPD_TX1_DN

UV9 (ESD3V3U4ULC) Dummy
V_DPD_TX0_DP 9 → 1 V_DPD_TX0_DP
V_DPD_TX0_DN 8 → 2 V_DPD_TX0_DN
3 GND
V_DPD_TX1_DP 7 → 4 V_DPD_TX1_DP
V_DPD_TX1_DN 6 → 5 V_DPD_TX1_DN

(12) V_DDSP_D_DP_2_DP — CV48 0.1uF 16V, X7R, +/-10% — V_DPD_TX2_DP
(12) V_DDSP_D_DP_2_DN — CV36 0.1uF 16V, X7R, +/-10% — V_DPD_TX2_DN
(12) V_DDSP_D_DP_3_DP — CV47 0.1uF 16V, X7R, +/-10% — V_DPD_TX3_DP
(12) V_DDSP_D_DP_3_DN — CV35 0.1uF 16V, X7R, +/-10% — V_DPD_TX3_DN

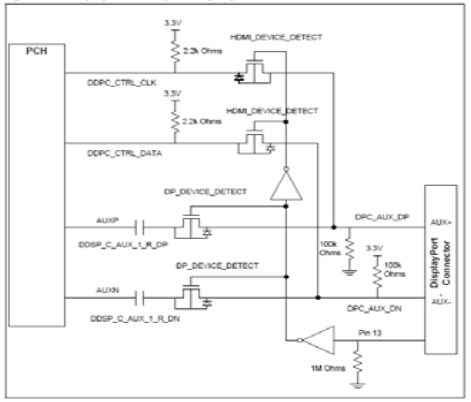
UV10 (ESD3V3U4ULC) Dummy
V_DPD_TX2_DP 9 → 1 V_DPD_TX2_DP
V_DPD_TX2_DN 8 → 2 V_DPD_TX2_DN
3 GND
V_DPD_TX3_DP 7 → 4 V_DPD_TX3_DP
V_DPD_TX3_DN 6 → 5 V_DPD_TX3_DN

UV7 (ESD3V3U4ULC) Dummy
V_DPD_AUX_DN 9 → 1 V_DPD_AUX_DN
V_DPD_AUX_DP 8 → 2 V_DPD_AUX_DP
3 GND
V_DPD_HPD_SINK 7 → 4 V_DPD_HPD_SINK
DPD_P13 6 → 5 DPD_P13

DP_PORT2 — CONN - Display port
23 HOLE3 HOLE2 22
1 ML_Lane0_P
2 GND1
3 ML_Lane0_N
4 ML_Lane1_P
5 GND2
6 ML_Lane1_N
7 ML_Lane2_P
8 GND3
9 ML_Lane2_N
10 ML_Lane3_P
11 GND4
12 ML_Lane3_N
13 GND5
14 GND6
15 AUX_CH_P
16 GND7
17 AUX_CH_N
18 H_P_DETECT
19 RETURN
20 DP_PWR
24 HOLE4 HOLE1 21

V_DPD_TX0_DP, V_DPD_TX0_DN, V_DPD_TX1_DP, V_DPD_TX1_DN, V_DPD_TX2_DP, V_DPD_TX2_DN, V_DPD_TX3_DP, V_DPD_TX3_DN, DPD_P13, V_DPD_AUX_DP, V_DPD_AUX_DN, V_DPD_HPD_SINK, V_DPD_PWR
RV53 1M
RV56 100K
Close to Connector

Figure 7-5. DisplayPort Interoperability Implementation



20110211:change 2N7002DW for cost down.

(24) V_DDSP_D_AUX_DN — CV44 0.1uF 16V, X7R, +/-10% — V_DDSP_D_AUX_DN_C
(24) V_DDSP_D_AUX_DP — CV41 0.1uF 16V, X7R, +/-10% — V_DDSP_D_AUX_DP_C

+3V — FV3 FUSE_1.1A — V_DPD_PWR
CV46 1uF 16V,X5R,+/-20%
CV34 10uF Dummy 10V,X5R,+/-20%
CV38 470pF 50V, X7R, +/-10%
CV40 22uF 6.3V,X5R,+/-20%

+3V — RV46 2.2K +/-5% — RV58 2.2K +/-5%
(24) V_DDPD_CTRL_CLK — V_DDPD_CTRL_CLK
(24) V_DDPD_CTRL_DATA — V_DDPD_CTRL_DATA

QV42 2N7002DW: V_DDPD_CTRL_CLK, DPD_P13_POS, V_DPD_AUX_DP — RV40 1M +/-5%
QV41 2N7002DW: V_DDPD_CTRL_DATA, DPD_P13_POS, V_DPD_AUX_DN — RV48 1M +/-5%
QV40 2N7002DW: V_DDSP_D_AUX_DP_C, DPD_P13_INV, V_DPD_AUX_DP — RV60 1M +/-5%
QV39 2N7002DW: V_DDSP_D_AUX_DN_C, DPD_P13_INV, V_DPD_AUX_DN — RV55 1M +/-5%

Display Port Hotplug Detect

+5V — RV51 1K Dummy — V_DPD_HPD_SINK
+5V — QV21 FDV301N (D, G, S) — RV44 100K
V_DDSP_D_HPD (22,24)

+3V — RV57 100KOhm +/-1%
+3V_DUAL — RV49 100KOhm +/-1% Dummy
+3V — RV52 100KOhm +/-1% Dummy
V_DPD_AUX_DN
V_DPD_AUX_DP
RV43 100KOhm +/-1% Dummy
RV45 100KOhm +/-1%

+5V — RV42 1K Dummy
DPD_P13 — RV47 8.2K +/-5% — CV39 0.1uF 16V, X7R, +/-10%
RV54 1M +/-5%

+12V — RV59 4.7K +/-5%
DPD_P13_INV
QV33 2N7002DW
+12V — RV41 8.2K +/-5% — DPD_P13_POS

20110211:change 2N7002DW for cost down.
20120312: delete RV50.

DELL INC.

Title: Display Port 2
DWG NO: Amazon USFF
Rev: A00
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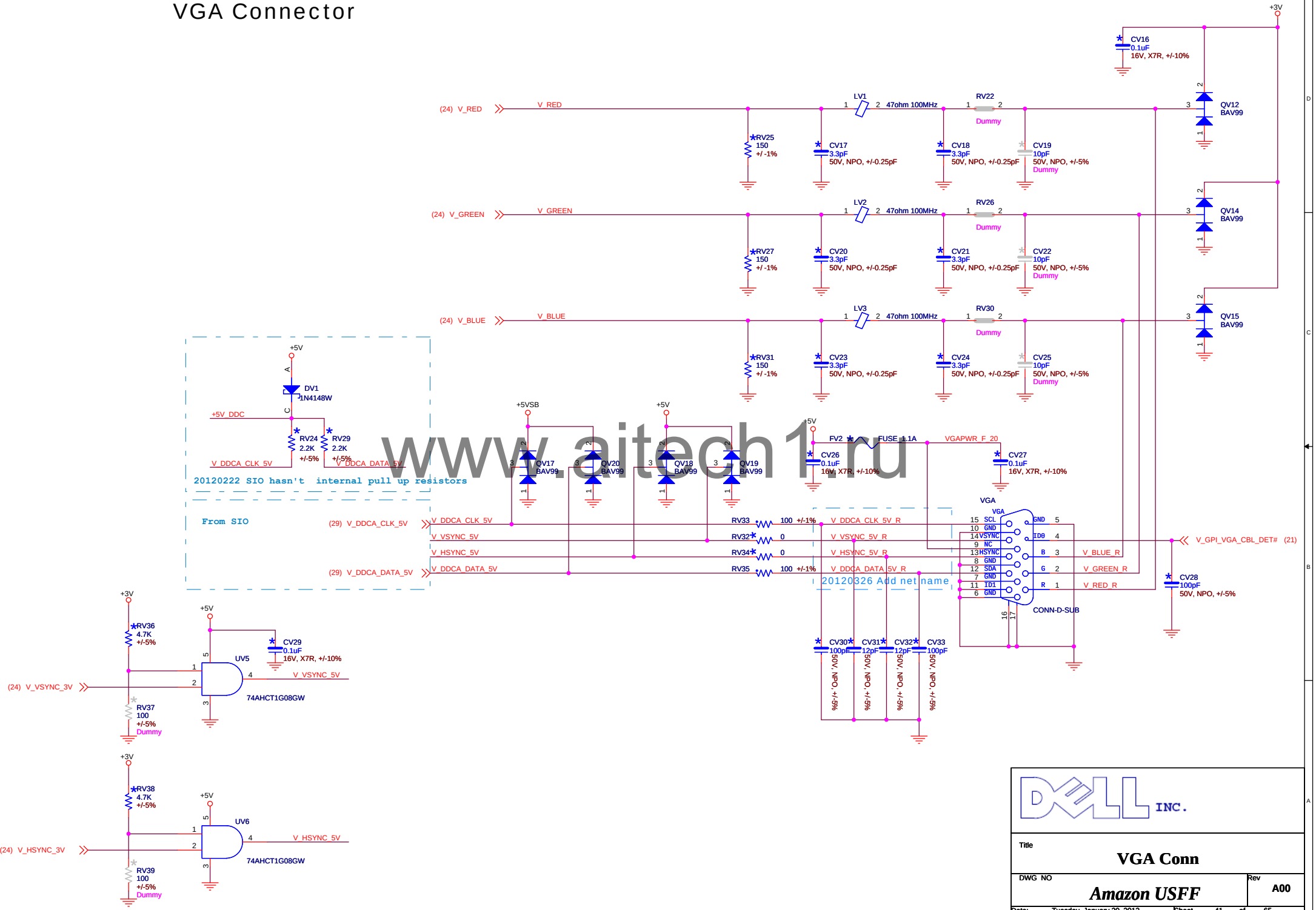
VGA Connector



DELL INC.

Title	VGA Conn
DWG NO	Amazon USFF
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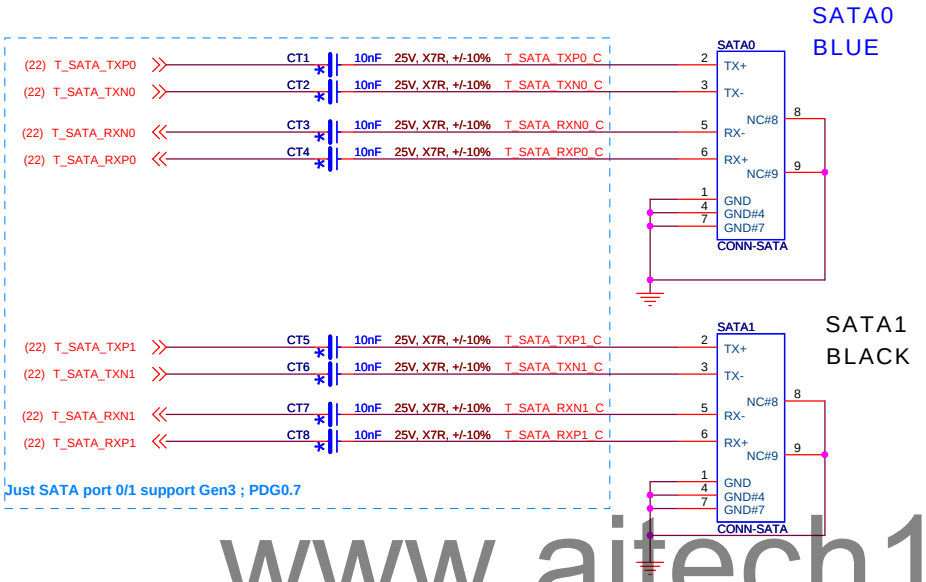
Date: Tuesday, January 29, 2013	Sheet 41 of 65



DELL INC.

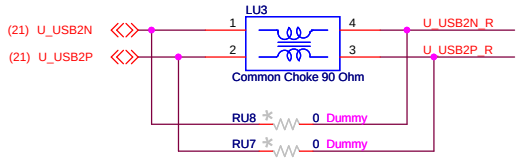
Title: **SATA Conn**

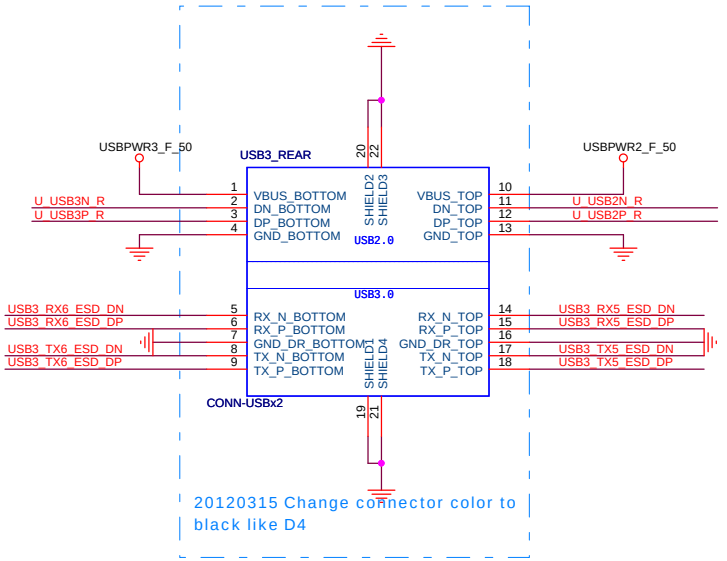
DWG NO: ***Amazon USFF***

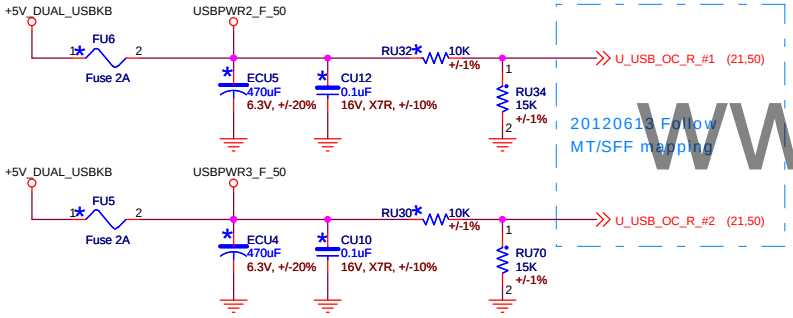
Rev: **A00**

Date: Tuesday, January 29, 2013 Sheet 42 of 65

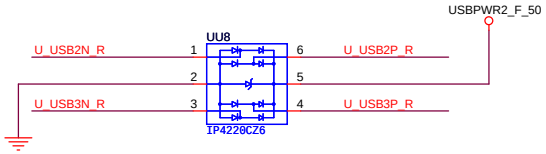
Rear USB 3.0 CONNECTOR

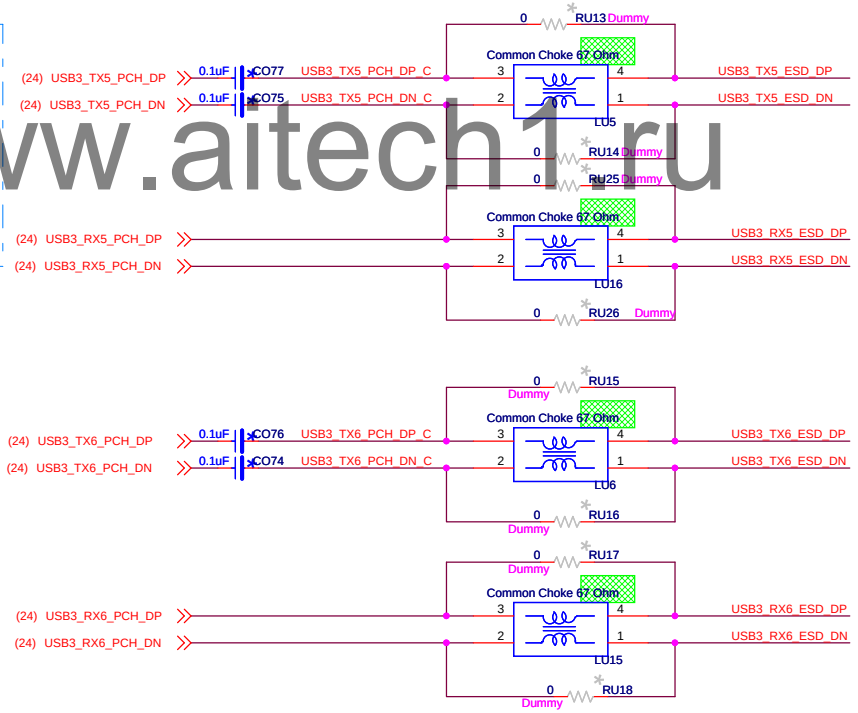




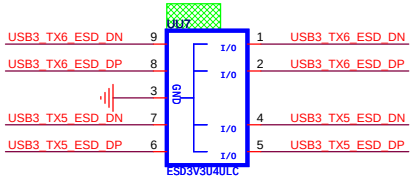


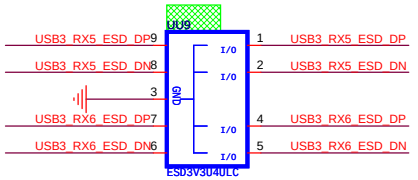
20120613 Follow MT/SFF mapping





Place ESD Close to Connector





DELL INC.

Title: **Rear USB3.0**

DWG NO: ***Amazon USFF***

Rev: **A00**

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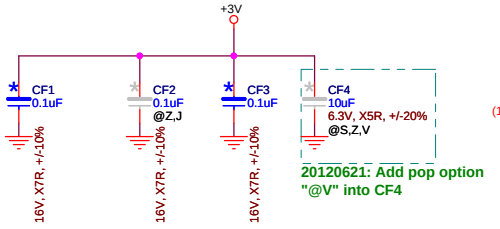
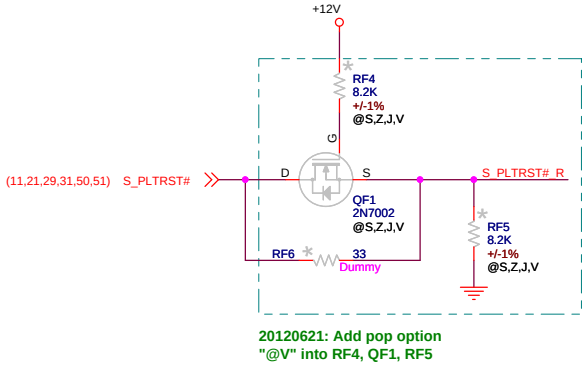
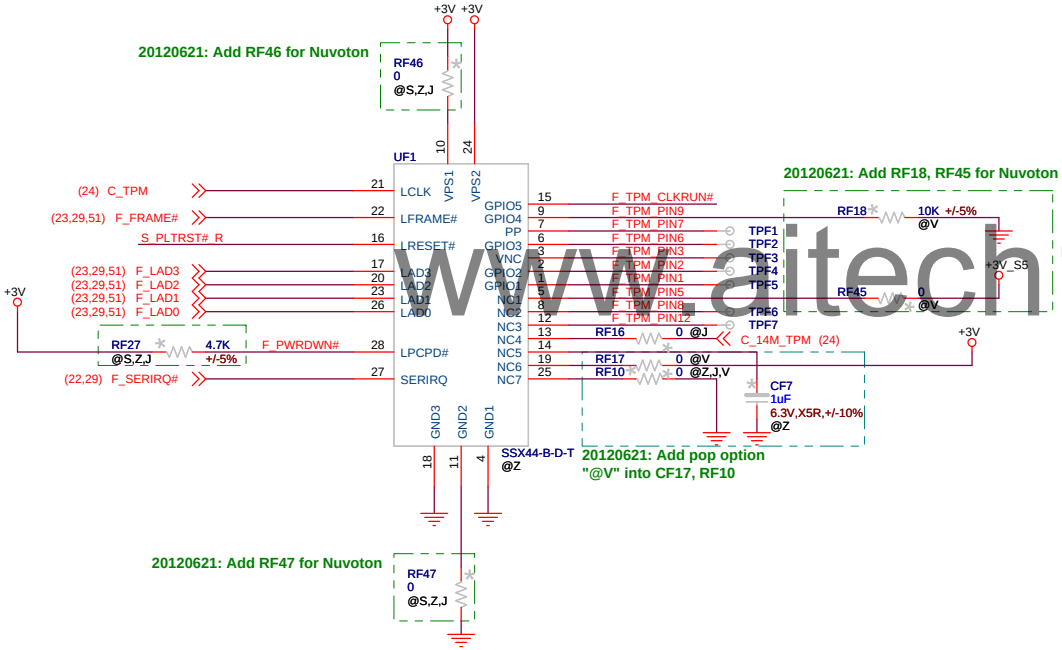
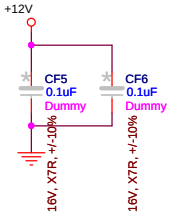
TPM, TCM (TCM is just reserved because MRD has removed TCM requirement)

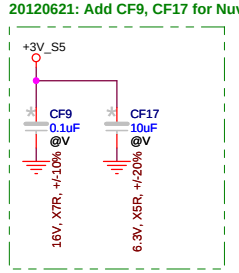
(Default) ST Micro	POP S	CF4
ZTE	POP Z	CF2,CF4,CF7,RF10,RF19,RF20,RF21
Jetway	POP J	CF2,CF8,RF10,RF16,RF21

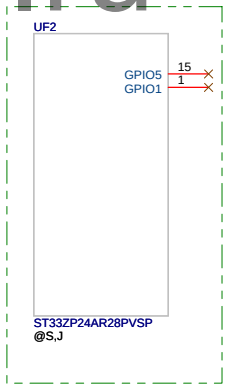


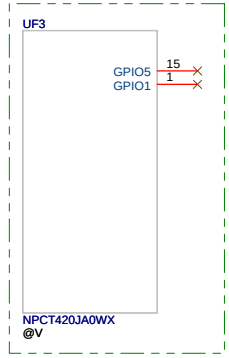


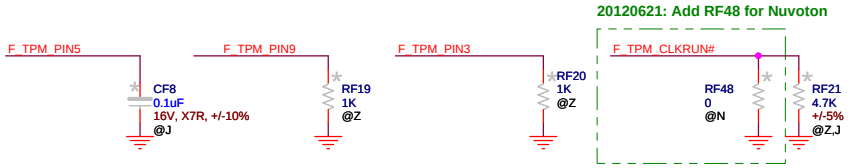












DELL INC.

Title: **TPM & TCM**

DWG NO: ***Amazon USFF***

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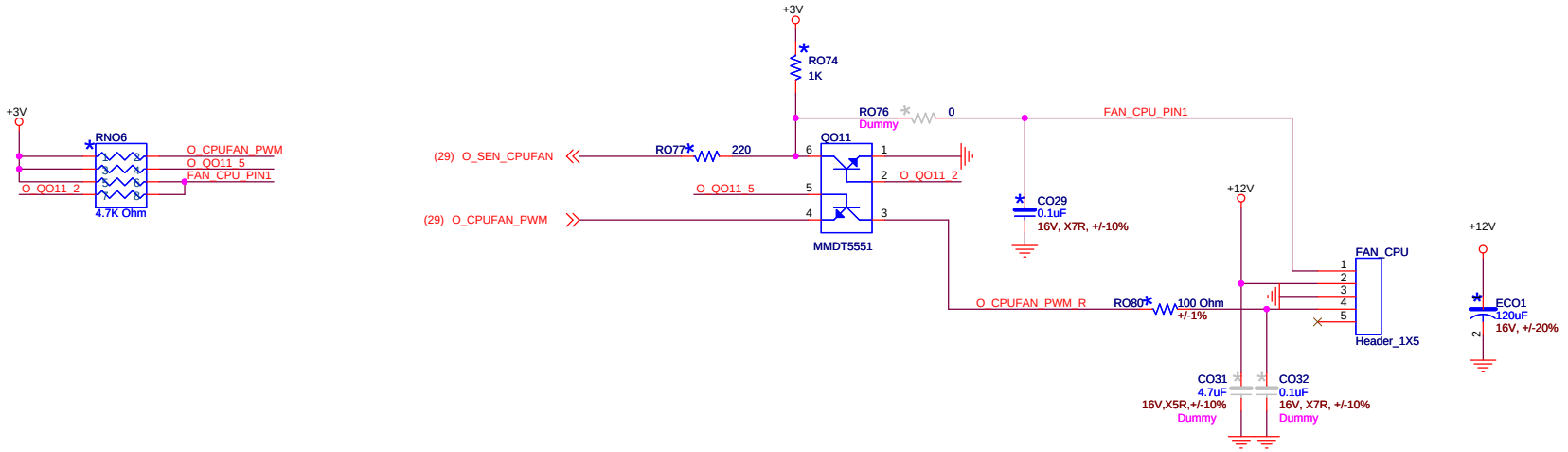
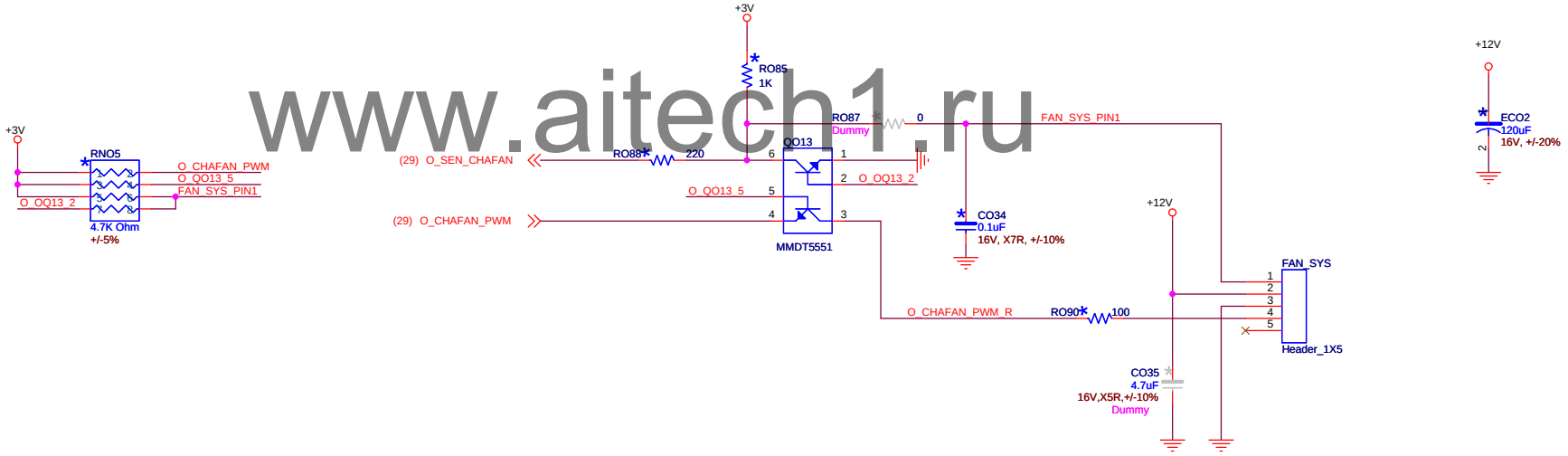
CPU Fan



SYS Fan



PSU Fan

DELL INC.

Title: **FAN**

DWG NO: ***Amazon USFF***

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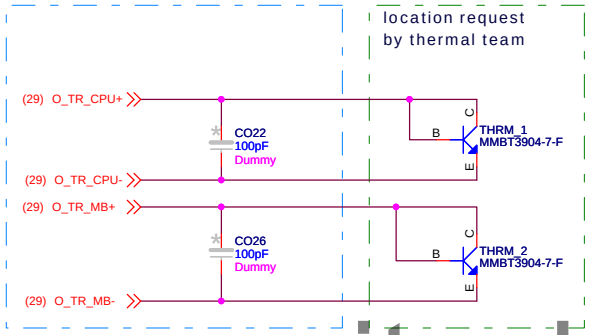

20100210: Swap CO24 and CO14 layout location
Swap CO23 and CO17 layout location

20100309: Dummy CO17,CO14

20100311: THRM2 reference name rename to THRM_1 , THRM3 reference name rename to THRM_2 , follow Dell PIG1.2

DELL INC.

Title: **Thermal Sensor**

DWG NO: ***Amazon USFF***

Rev: **A00**

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KB/MS

DELL INC.

Title

PS2 Conn

DWG NO

Amazon USFF

Rev

A00

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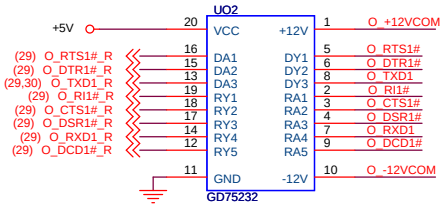
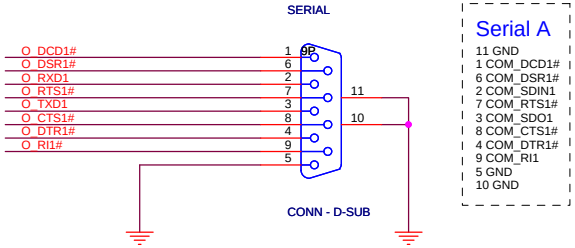
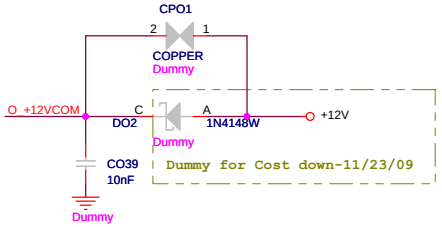
Serial Port 1

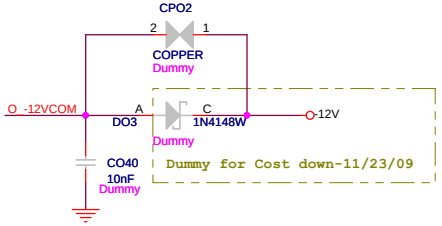




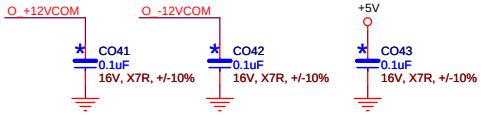
Serial A

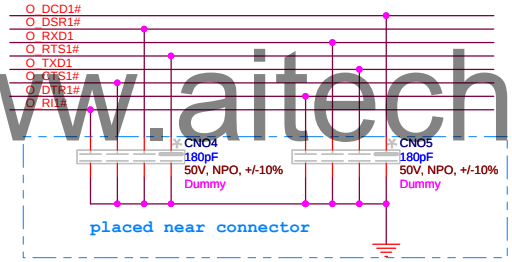
11 GND
1 COM_DCD1#
6 COM_DSR1#
2 COM_SDIN1
7 COM_RTS1#
3 COM_SDO1
8 COM_CTS1#
4 COM_DTR1#
9 COM_RI1
5 GND
10 GND





placed near UO2





DELL INC.

Title

COM1

DWG NO

Amazon USFF

Rev

A00

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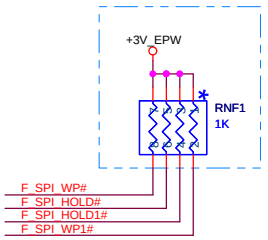
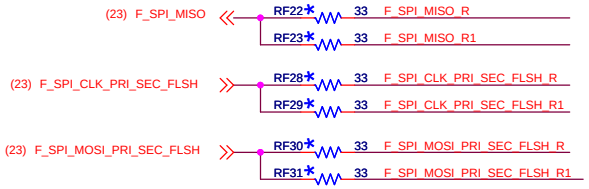
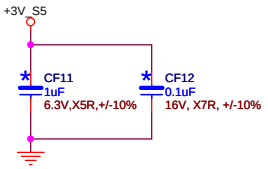
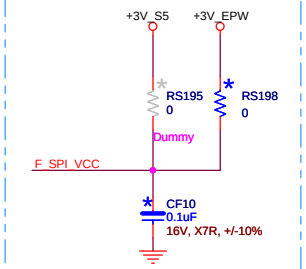
20120515: RNF1 pull-up change to +3V_EPW







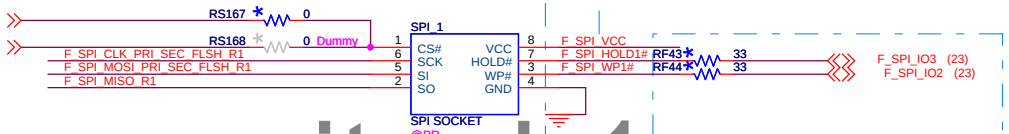
20120515: Add RS195, RS198 for SPI ROM option.



SPI_4MB

20120515: change net name to F_SPI_VCC

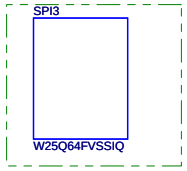
20110530: SPI1 Change to 4M
20120216: SPI1 Change to WINBOND_W25Q32BVSSIG
2012020917: SPI1 Change to WINBOND_W25Q32FVSSIQ
2012021024: UPDATE WINBOND_W25Q32FVSSIQ VPN

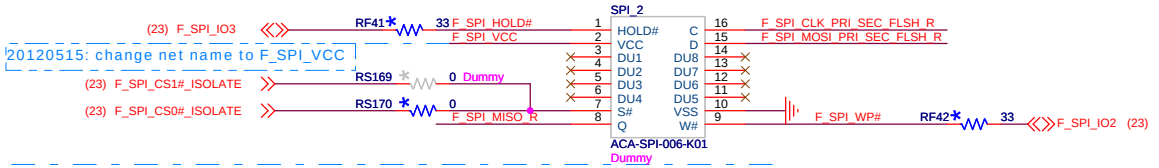


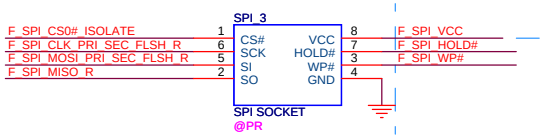
20120306 Add RF43,44

SPI_8MB

20120216: SPI2 rename to SPI3 and Change to 8M , 8 pins flash
20120216: SPI3 and Change to 8M , 8 pins flash, WINBOND_W25Q64FVSSIG
20120917: SPI1 Change to WINBOND_W25Q64FVSSIQ
2012021024: UPDATE VPN







20120515: change net name to F_SPI_VCC

DELL INC.

Title: **SPI**

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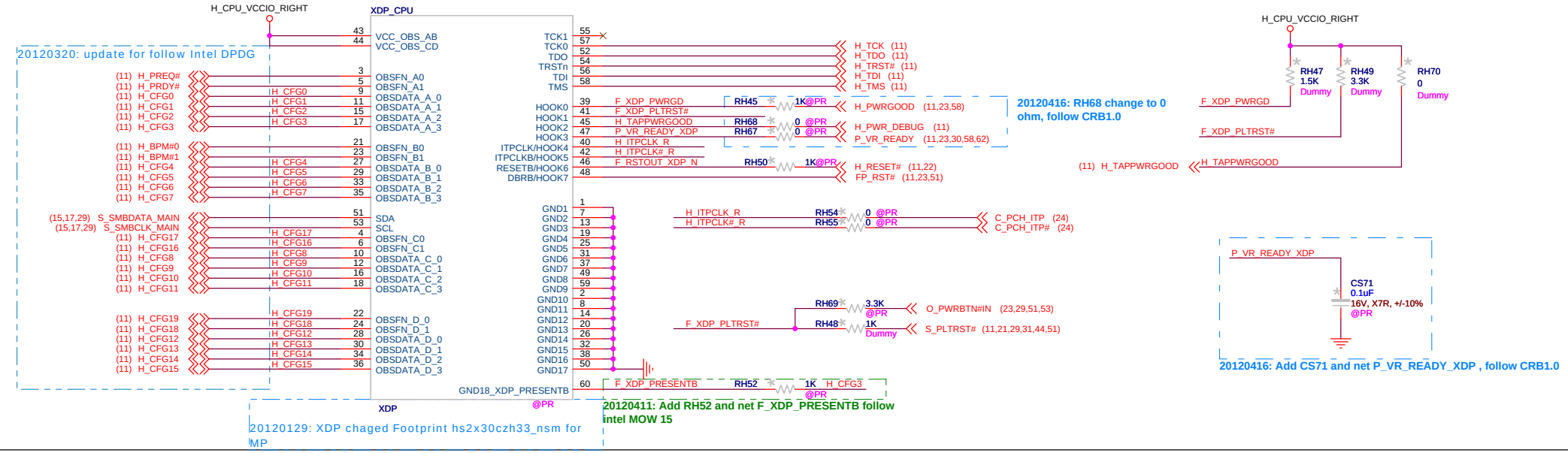
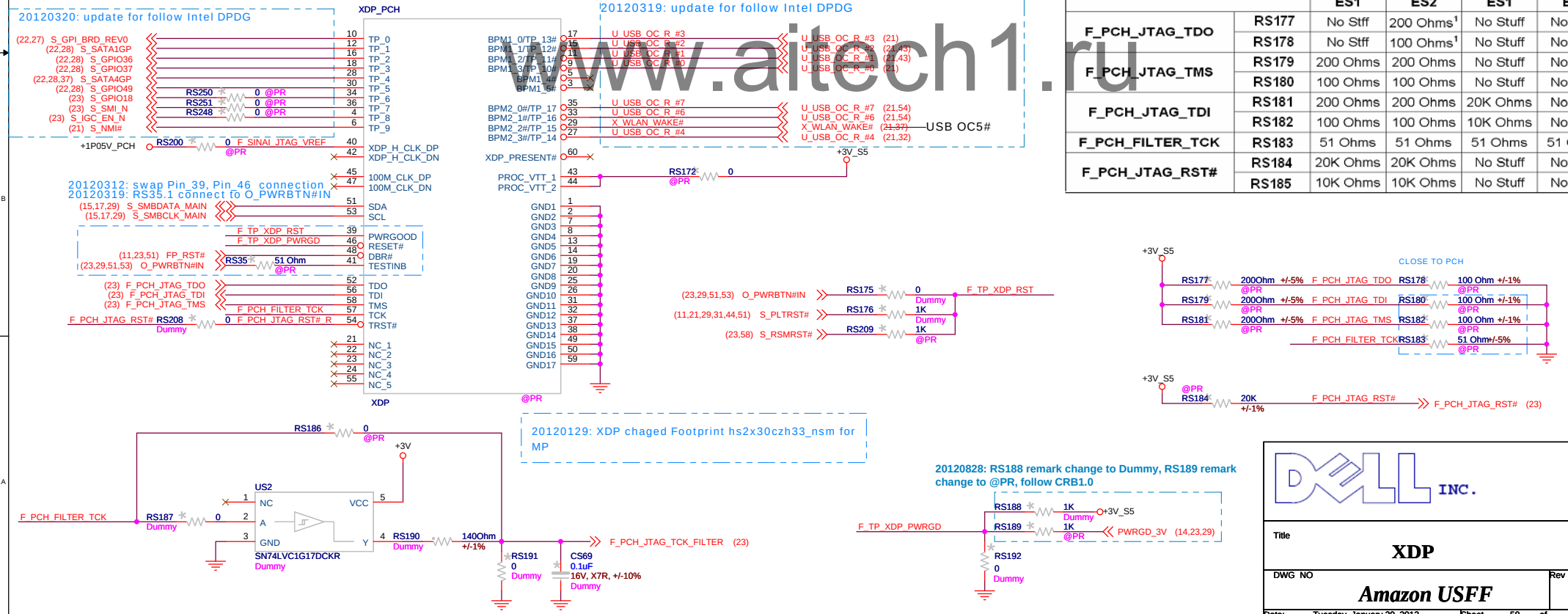
XDP Connector - CPU



XDP Connector - PCH



2009/12/21 Update JTAG Table		PCH JTAG Enable		PCH JTAG Disable	
		ES1	ES2	ES1	ES2
F_PCH_JTAG_TDO	RS177	No Stff	200 Ohms[1]	No Stuff	No Stuff
	RS178	No Stff	100 Ohms[1]	No Stuff	No Stuff
F_PCH_JTAG_TMS	RS179	200 Ohms	200 Ohms	No Stuff	No Stuff
	RS180	100 Ohms	100 Ohms	No Stuff	No Stuff
F_PCH_JTAG_TDI	RS181	200 Ohms	200 Ohms	20K Ohms	No Stuff
	RS182	100 Ohms	100 Ohms	10K Ohms	No Stuff
F_PCH_FILTER_TCK	RS183	51 Ohms	51 Ohms	51 Ohms	51 Ohms
F_PCH_JTAG_RST#	RS184	20K Ohms	20K Ohms	No Stuff	No Stuff
	RS185	10K Ohms	10K Ohms	No Stuff	No Stuff

DELL INC.

Title: XDP

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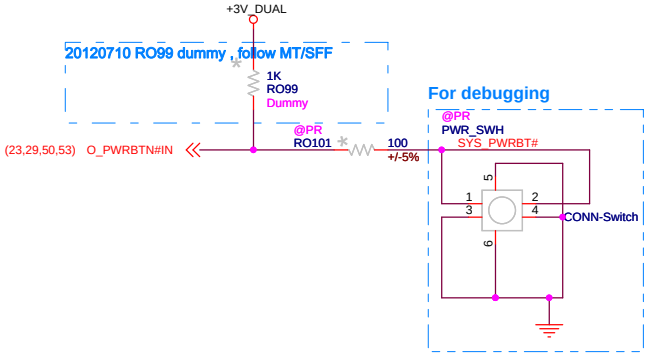
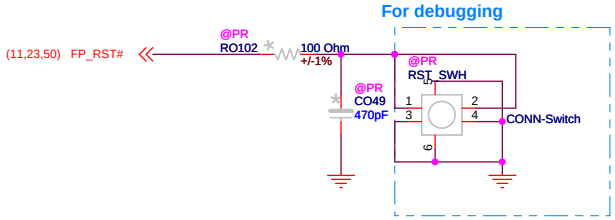
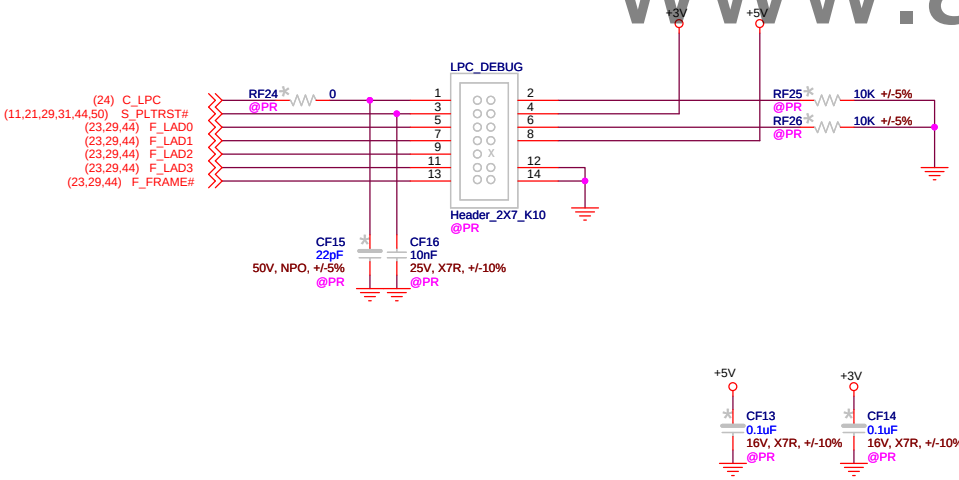
Power Bottom



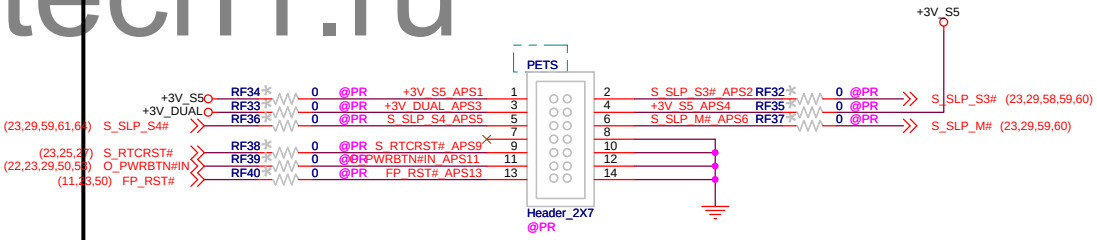
Reset Bottom



LPC DEBUG



APS Connector



DELL INC.

Title: **Pilot Run Conn**

DWG NO: ***Amazon USFF***

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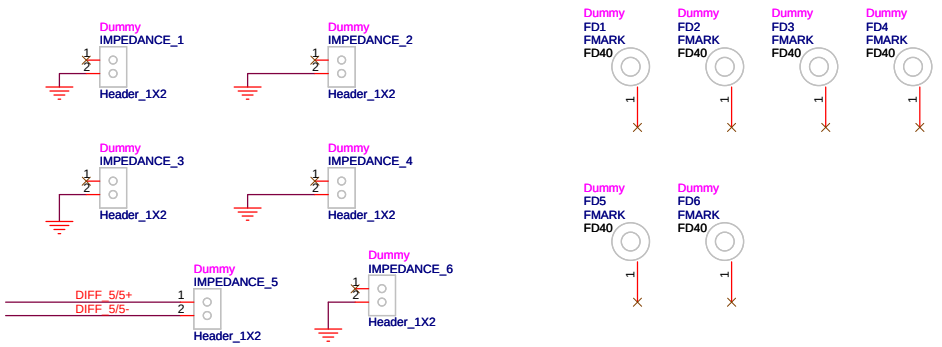

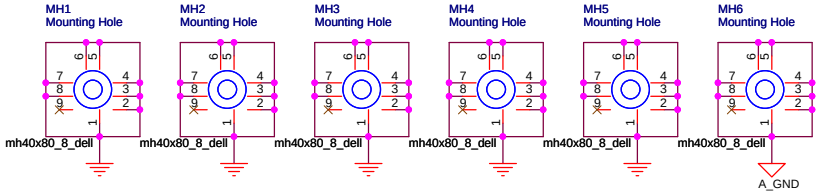

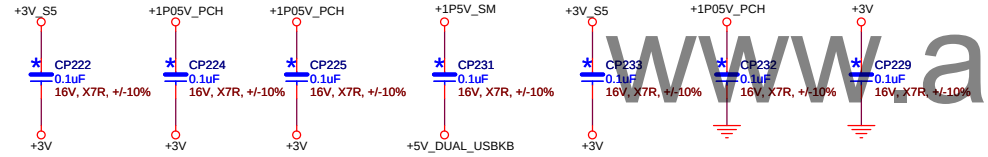

DELL INC.

Title

EMI

DWG NO

Amazon USFF

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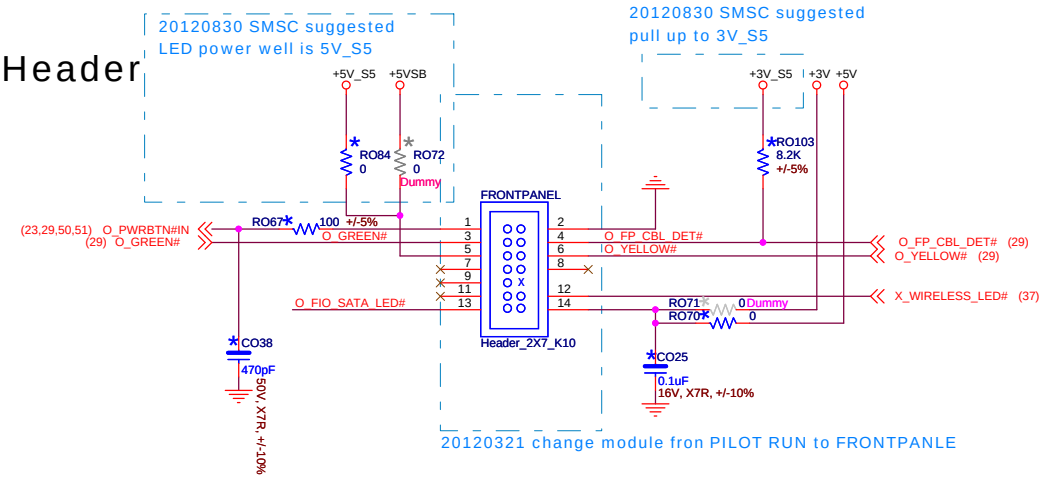
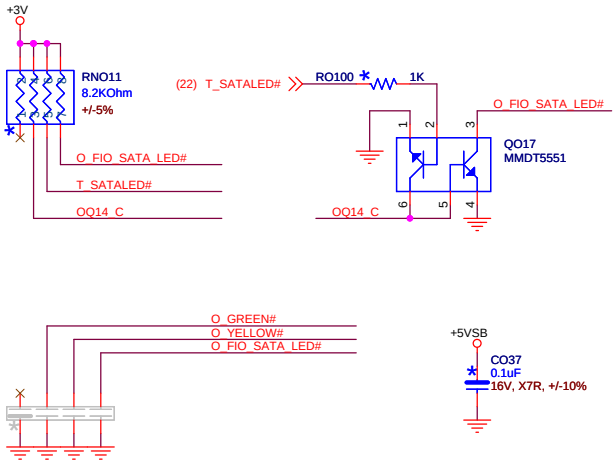
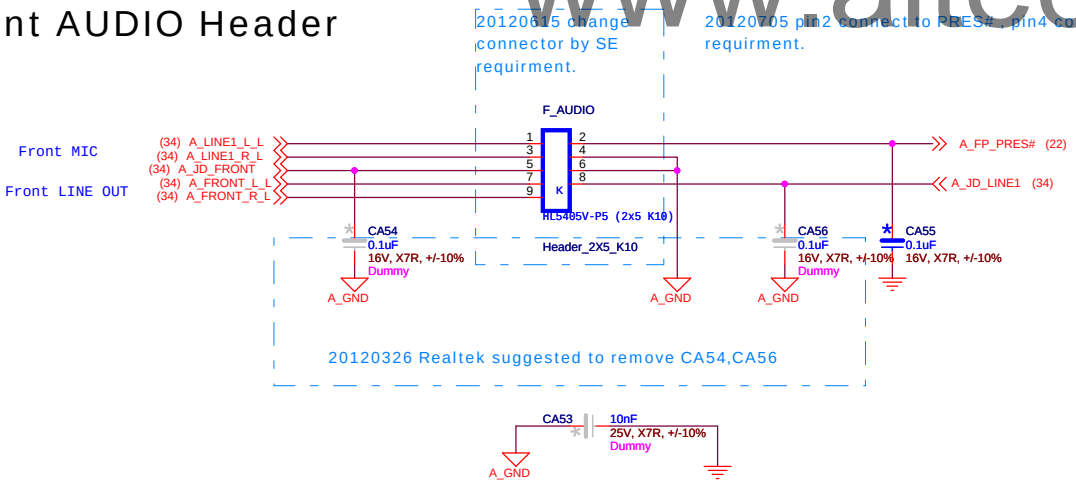
FRONTPANEL Header





Front AUDIO Header



DELL INC.

Title: **Front_Panel**

DWG NO: ***Amazon USFF***

Rev: **A00**

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Front USB/LED Header

20120214: USB3_FRONT connector change to PUB200-2017-B5-10-HF.
20121225: USB3_FRONT update VPN

USBPWR1_F_50
USBPWR0_F_50
USB3_FRONT
PUB200-2017-B5-10-HF

USB3_RX2_ESD_DN
USB3_RX2_ESD_DP
USB3_TX2_ESD_DN
USB3_TX2_ESD_DP
U_USB13N_R
U_USB13P_R
USB3_RX1_ESD_DN
USB3_RX1_ESD_DP
USB3_TX1_ESD_DN
USB3_TX1_ESD_DP
U_USB12N_R
U_USB12P_R

+5V_DUAL_USBKB
CU5 0.1uF 16V, X7R, +/-10%

+3V
RU40 8.2K +/-5%
(22) S_USB_HDR_DET#

20120220 Folow MT /SFF USB mapping

+5V_DUAL_USBKB
USBPWR0_F_50
FU10 Fuse 2A
ECU7 470uF 6.3V, +/-20%
CU19 0.1uF 16V, X7R, +/-10% Dummy
RU66 10K +/-1%
RU72 15K +/-1%
U_USB_OC_R_#6 (21,50)

+5V_DUAL_USBKB
USBPWR1_F_50
FU7 Fuse 2A
CU20 0.1uF 16V, X7R, +/-10% Dummy
RU54 10K +/-1%
RU58 15K +/-1%
U_USB_OC_R_#7 (21,50)

20120315 Folow D4 USFF design

20120301 Swap pin for layout routing

20120614 PDG1.0 suggested move AC caps to FIO board

Place ESD Close to Header

(24) USB3_TX1_PCH_DN
(24) USB3_TX1_PCH_DP
RU53 0
Common Choke 67 Ohm
LU20 Dummy
RU49 0
USB3_TX1_ESD_DN
USB3_TX1_ESD_DP

(24) USB3_RX1_PCH_DN
(24) USB3_RX1_PCH_DP
RU57 0
Common Choke 67 Ohm
LU21 Dummy
RU60 0
USB3_RX1_ESD_DN
USB3_RX1_ESD_DP

20120614 PDG1.0 suggested move AC caps to FIO board

(24) USB3_TX2_PCH_DN
(24) USB3_TX2_PCH_DP
RU46 0
Common Choke 67 Ohm
LU18 Dummy
RU56 0
USB3_TX2_ESD_DN
USB3_TX2_ESD_DP

(24) USB3_RX2_PCH_DN
(24) USB3_RX2_PCH_DP
RU45 0
Common Choke 67 Ohm
LU17 Dummy
RU47 0
USB3_RX2_ESD_DN
USB3_RX2_ESD_DP

20120314 Follow D4 design
Dummy them on both MB and FIO

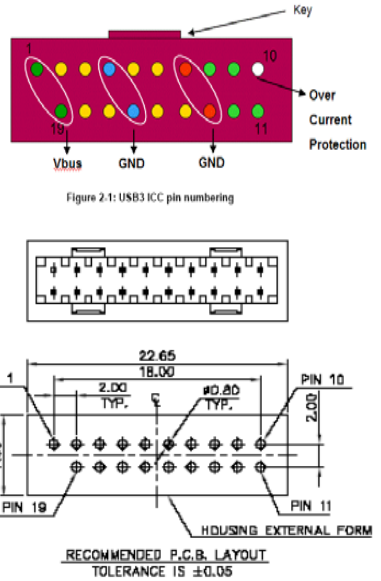


Figure 2-1: USB3 ICC pin numbering

(21) U_USB12P
(21) U_USB12N
LU19
Common Choke 90 Ohm
RU55 0 Dummy
RU59 0 Dummy
U_USB12P_R
U_USB12N_R

(21) U_USB13P
(21) U_USB13N
LU22
Common Choke 90 Ohm
RU48 0 Dummy
RU50 0 Dummy
U_USB13P_R
U_USB13N_R

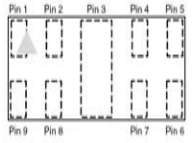
20120309 EMC suggested ESD stuff on FIO board

U_USB13N_R
U_USB12P_R
UU12
IP4220CZ6
Dummy
U_USB13P_R
U_USB12N_R
USBPWR1_F_50

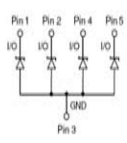
20120301 Swap pin for layout routing

USB3_TX1_ESD_DP
USB3_TX1_ESD_DN
USB3_TX2_ESD_DP
USB3_TX2_ESD_DN
UU10
ESD3V3U4ULC
Dummy
USB3_TX1_ESD_DP
USB3_TX1_ESD_DN
USB3_TX2_ESD_DP
USB3_TX2_ESD_DN

USB3_RX1_ESD_DP
USB3_RX1_ESD_DN
USB3_RX2_ESD_DP
USB3_RX2_ESD_DN
UU11
ESD3V3U4ULC
Dummy
USB3_RX1_ESD_DP
USB3_RX1_ESD_DN
USB3_RX2_ESD_DP
USB3_RX2_ESD_DN



a) Pin configuration



b) Schematic diagram

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DELL INC.

Title

SATA_MT

DWG NO

Amazon USFF

Rev

A00

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FLEXBAY

DELL INC.

Title

Flexbay USB_MT

DWG NO

Amazon USFF

Rev

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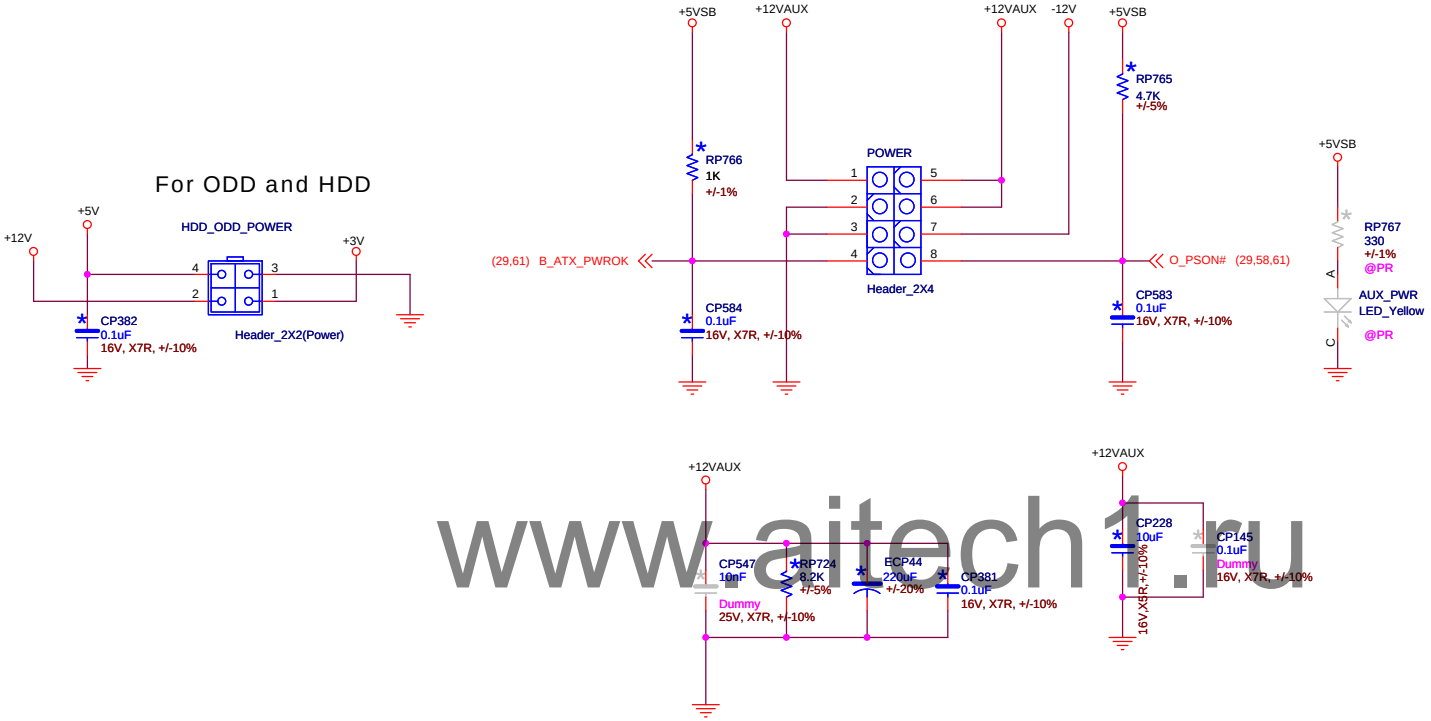
ATX POWER CONNECTOR



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Title

Power Conn

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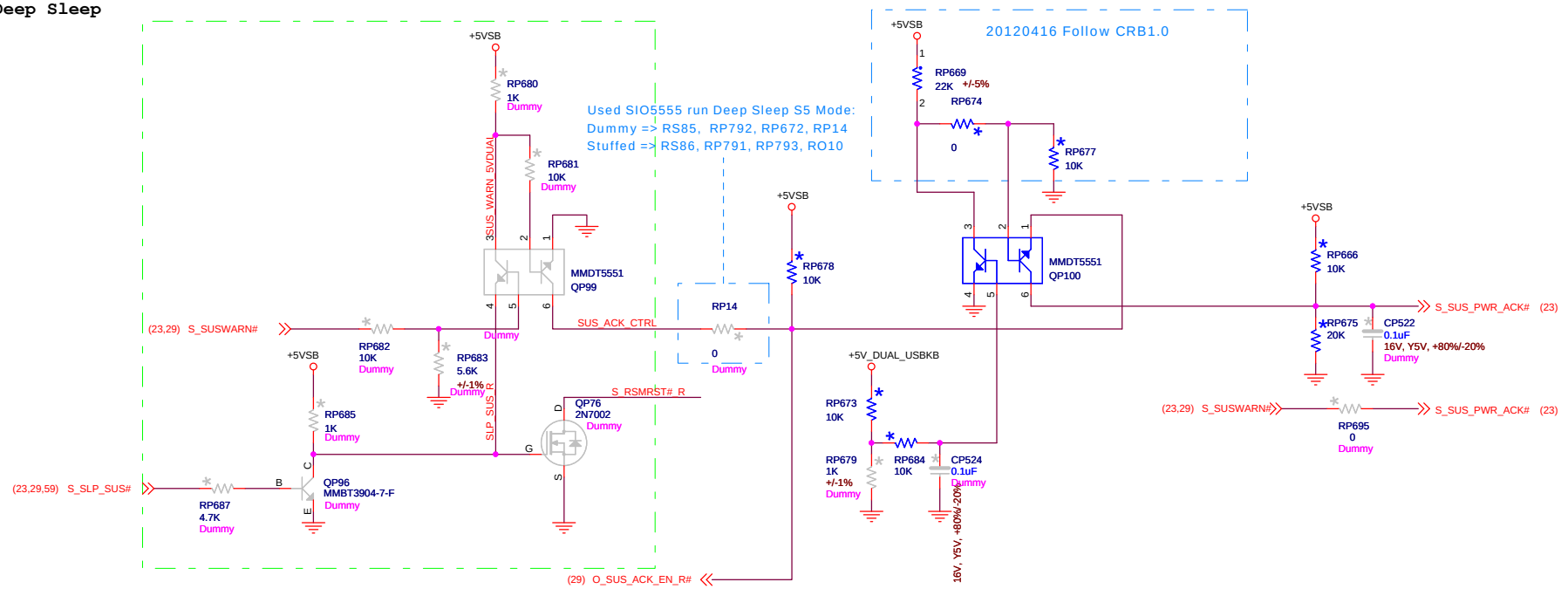
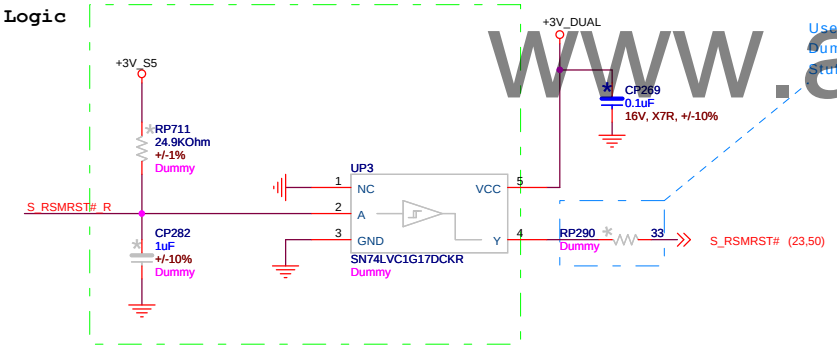
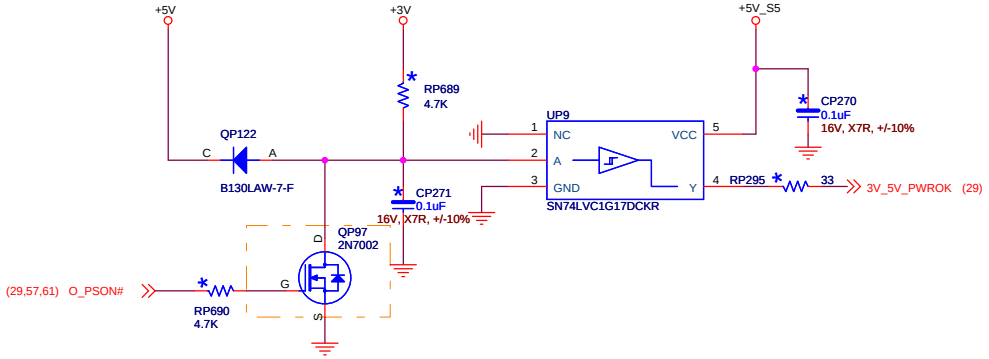
For Deep Sleep



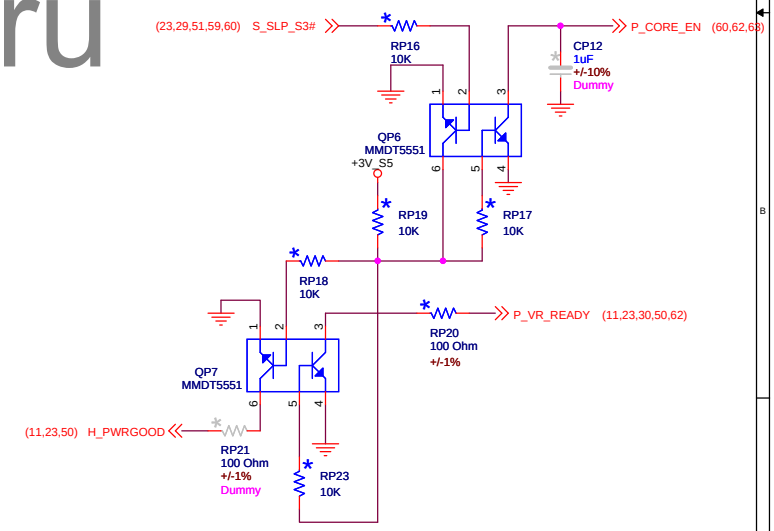
RESUME RESET Logic



New ATXPWROK



VR_READY DEFENSIVE



DELL INC.

Title: **Power Sequence**

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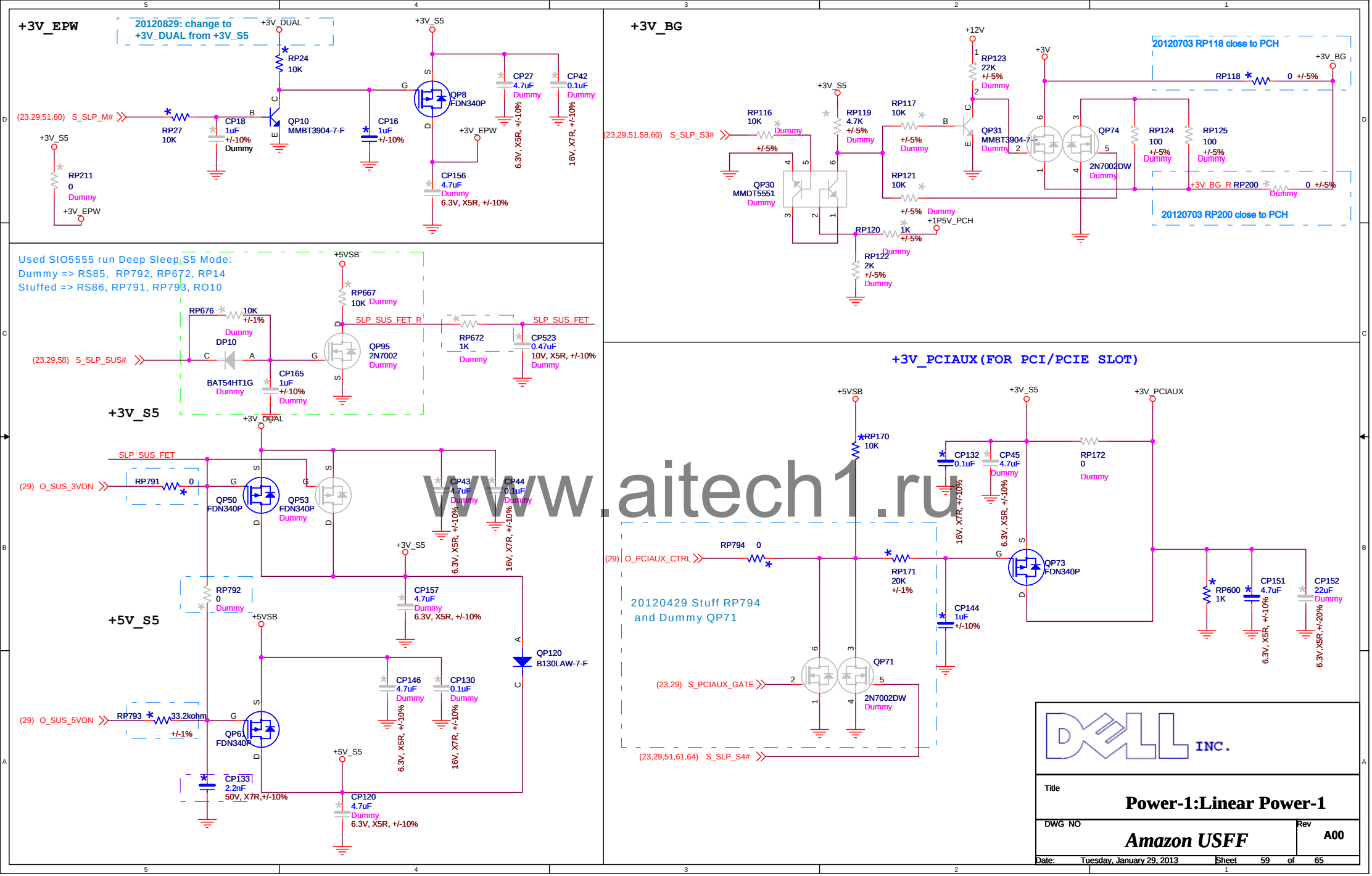
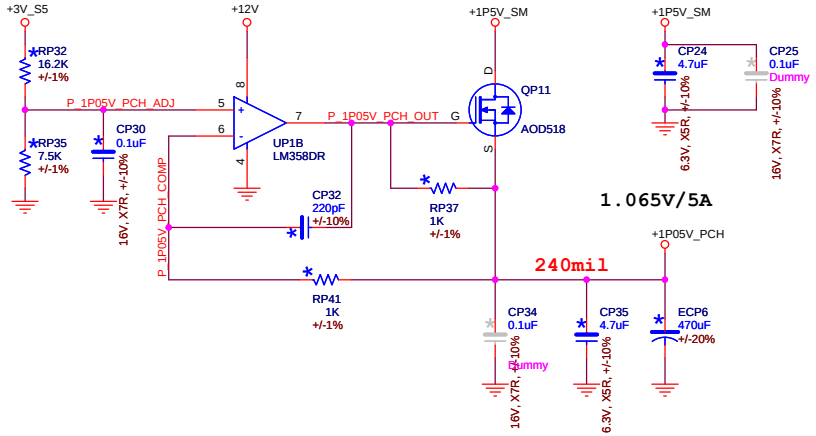
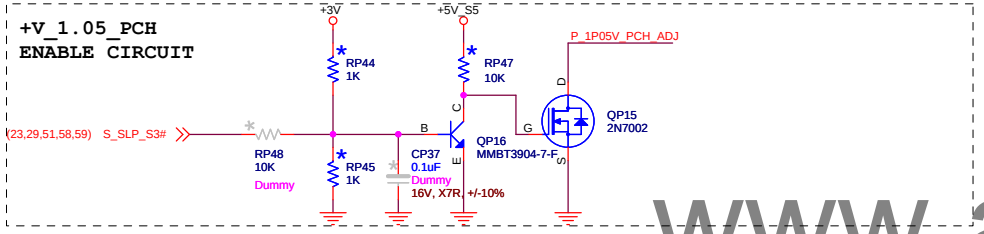


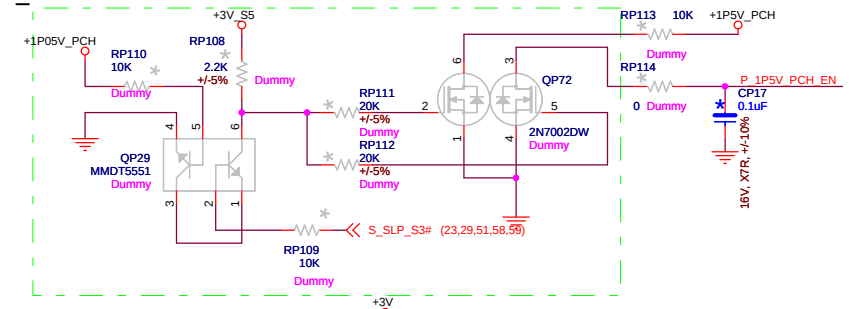
+V_1.05_PCH

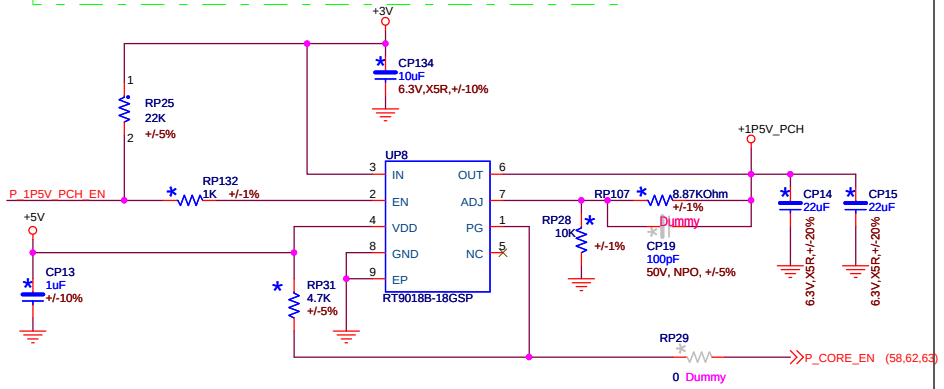


+V_1.05_PCH ENABLE CIRCUIT

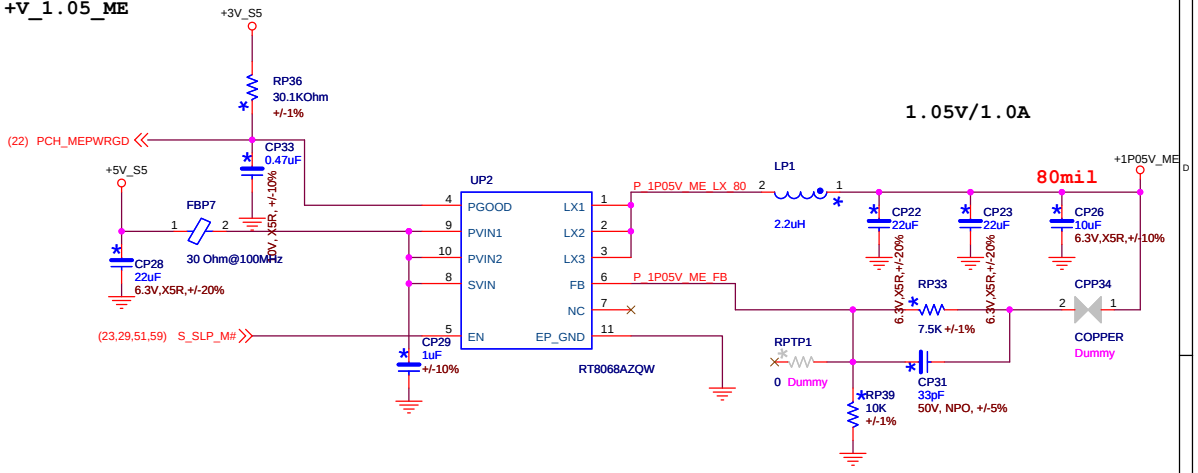


+V_1P5_PCH





+V_1.05_ME



DELL INC.

Title: **Power-2:Linear Power-2**

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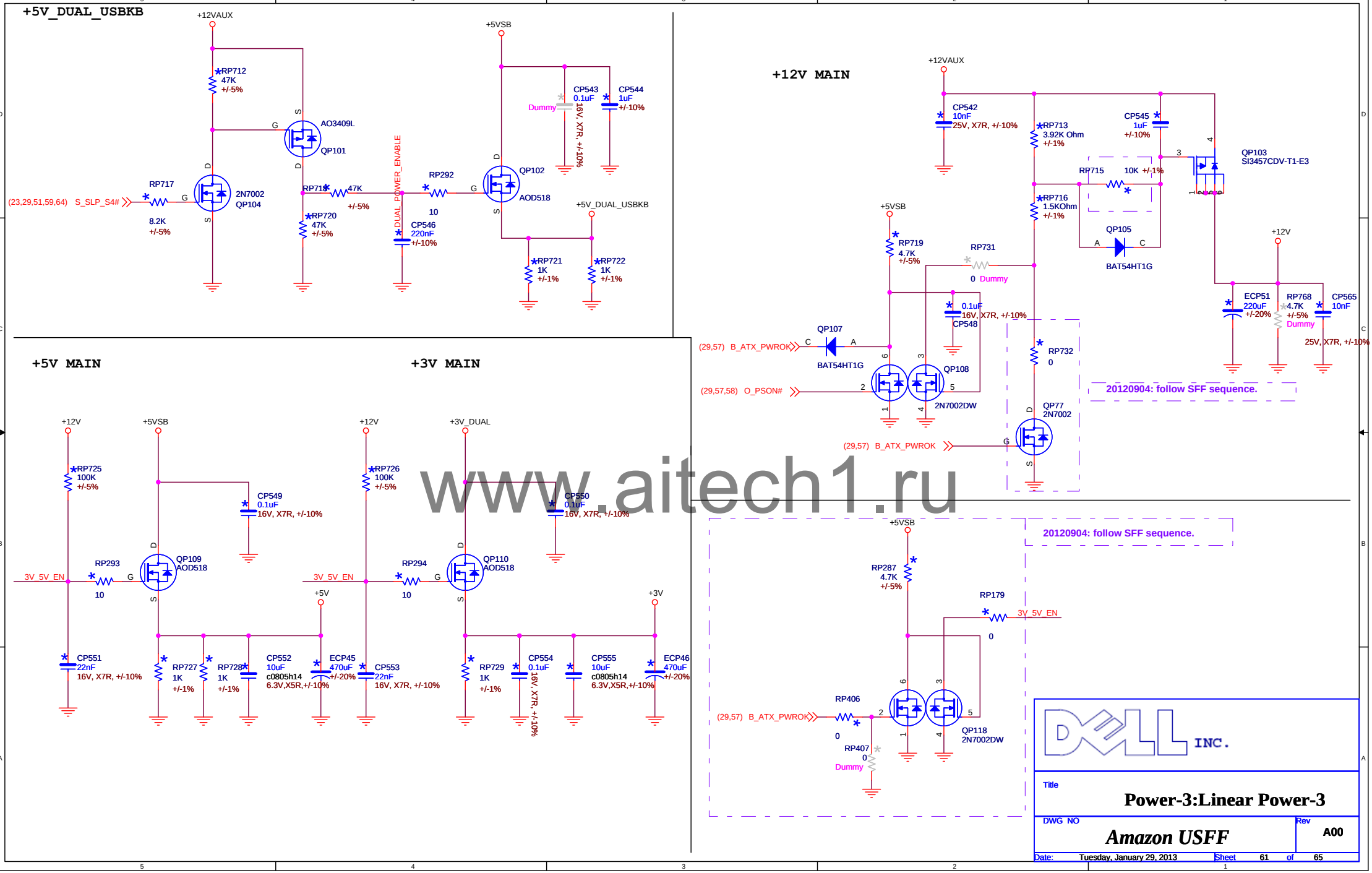
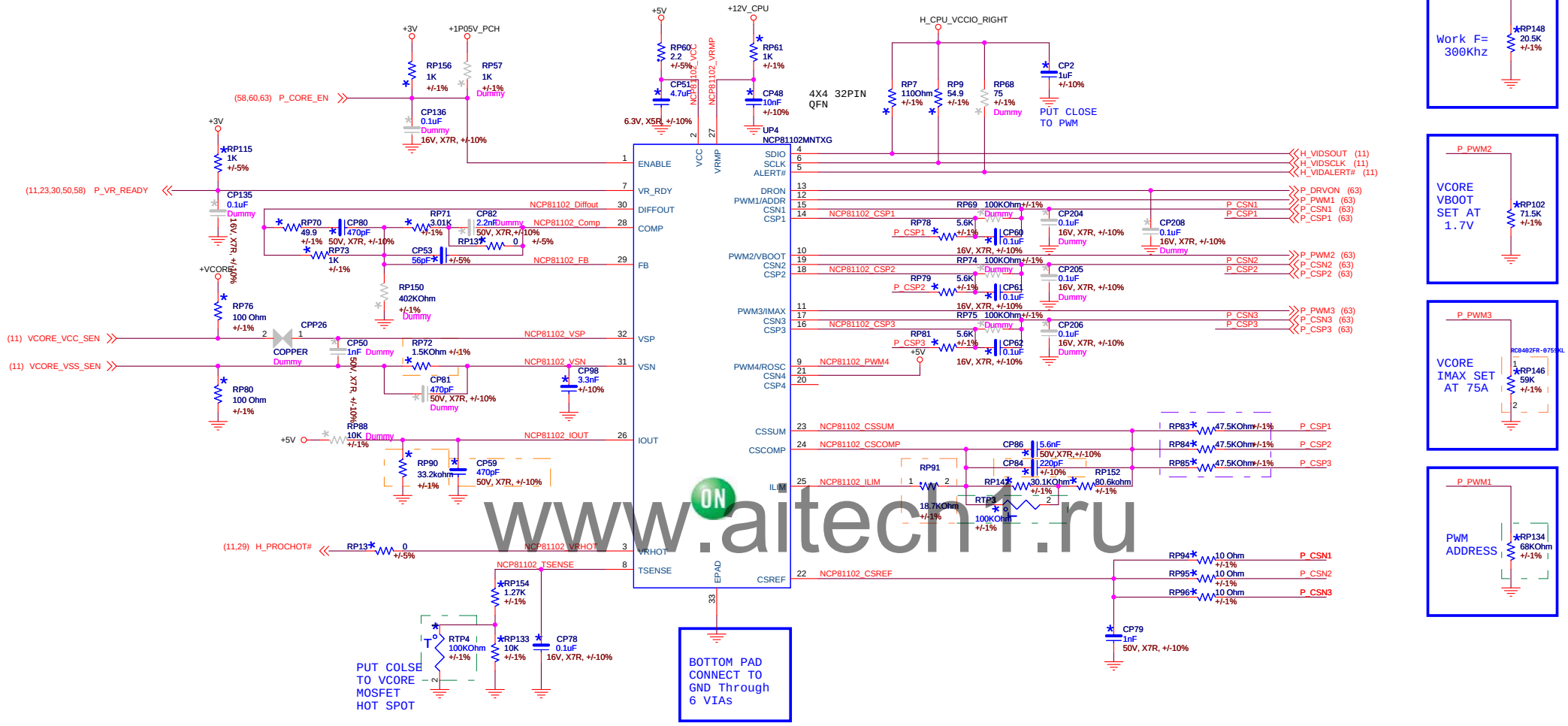


SharkBay VR12.5 POWER CKT -3PHASE



Rosc	Freq.	Rosc	Freq.	Rosc	Freq.	Rosc	Freq.	Rosc	Freq.
10K	250Kh	30.9K	340Khz	61.9K	430Khz	105K	520 Khz	165K	610Khz
12K	260Kh	34K	350Khz	64.9K	440Khz	110K	530Khz	174K	620Khz
14K	270Kh	36.5K	360Khz	69.8K	450Khz	115K	540Khz	182K	630Khz
16.2K	280Kh	40.2K	370Khz	73.2K	460Khz	121K	550Khz	191K	640Khz
18.2K	290Kh	43.2K	380Khz	78.7K	470Khz	130K	560Khz	200K	650Khz
20.5K	300Kh	46.4K	390Khz	82.5K	480Khz	137K	570Khz		
23.2K	310Kh	49.9K	400Khz	88.7K	490Khz	143K	580Khz		
25.5K	320Kh	53.6K	410Khz	93.1K	500Khz	150 K	590Khz		
28K	330Kh	57.6K	420Khz	100K	510Khz	158 K	600Khz		

DELL INC.

Title: **Power-4:VCore**

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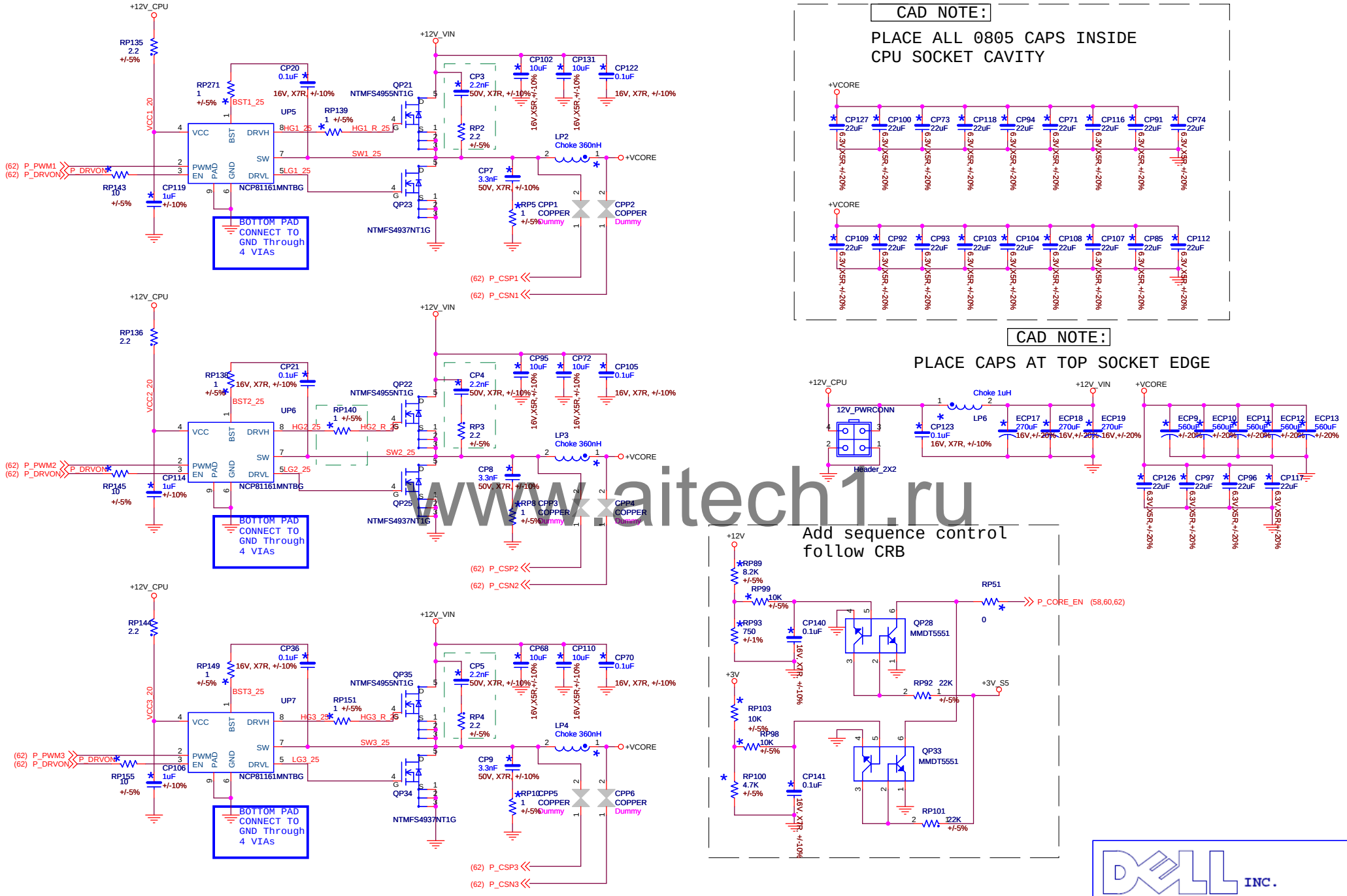
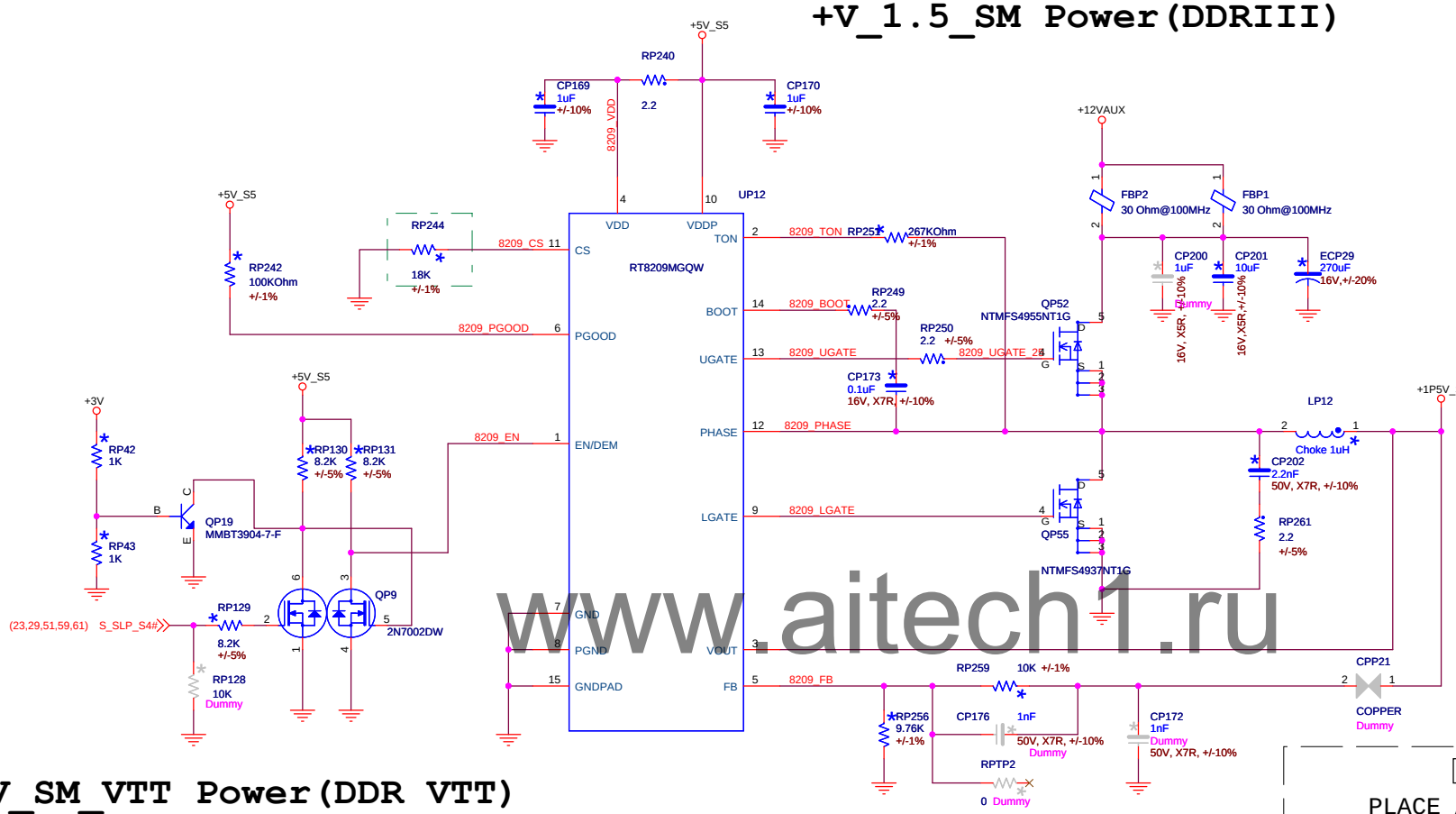
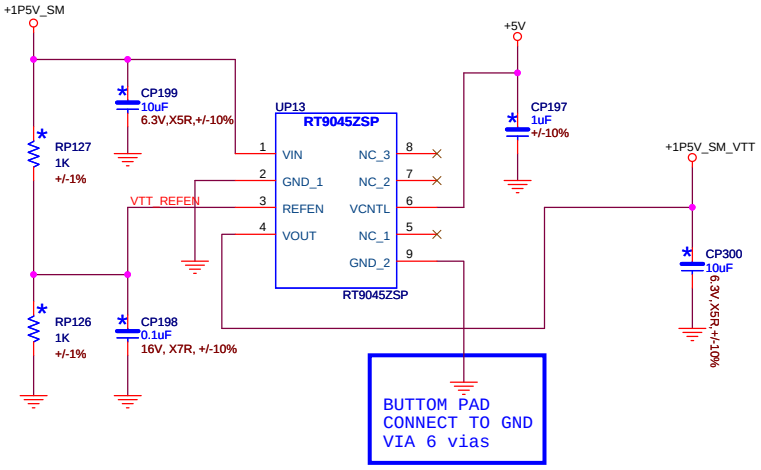
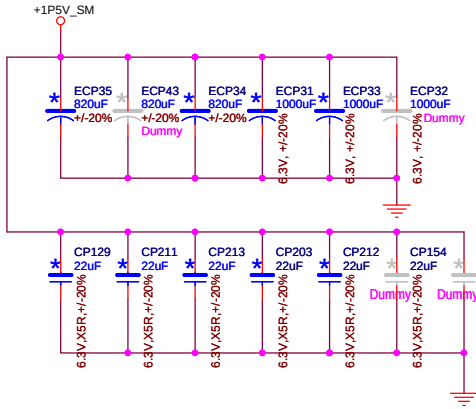


+V_1.5_SM Power(DDRIII)



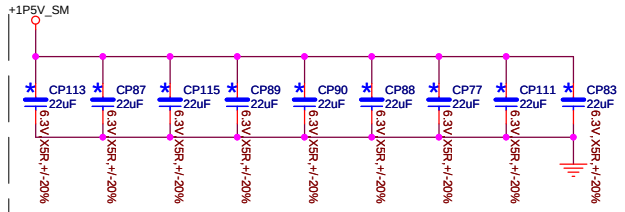
+V_SM_VTT Power(DDR VTT)





CAD NOTE:

PLACE ALL 0805 CAPS INSIDE
CPU SOCKET CAVITY



DELL INC.

Title: **Power-6: DDR3**

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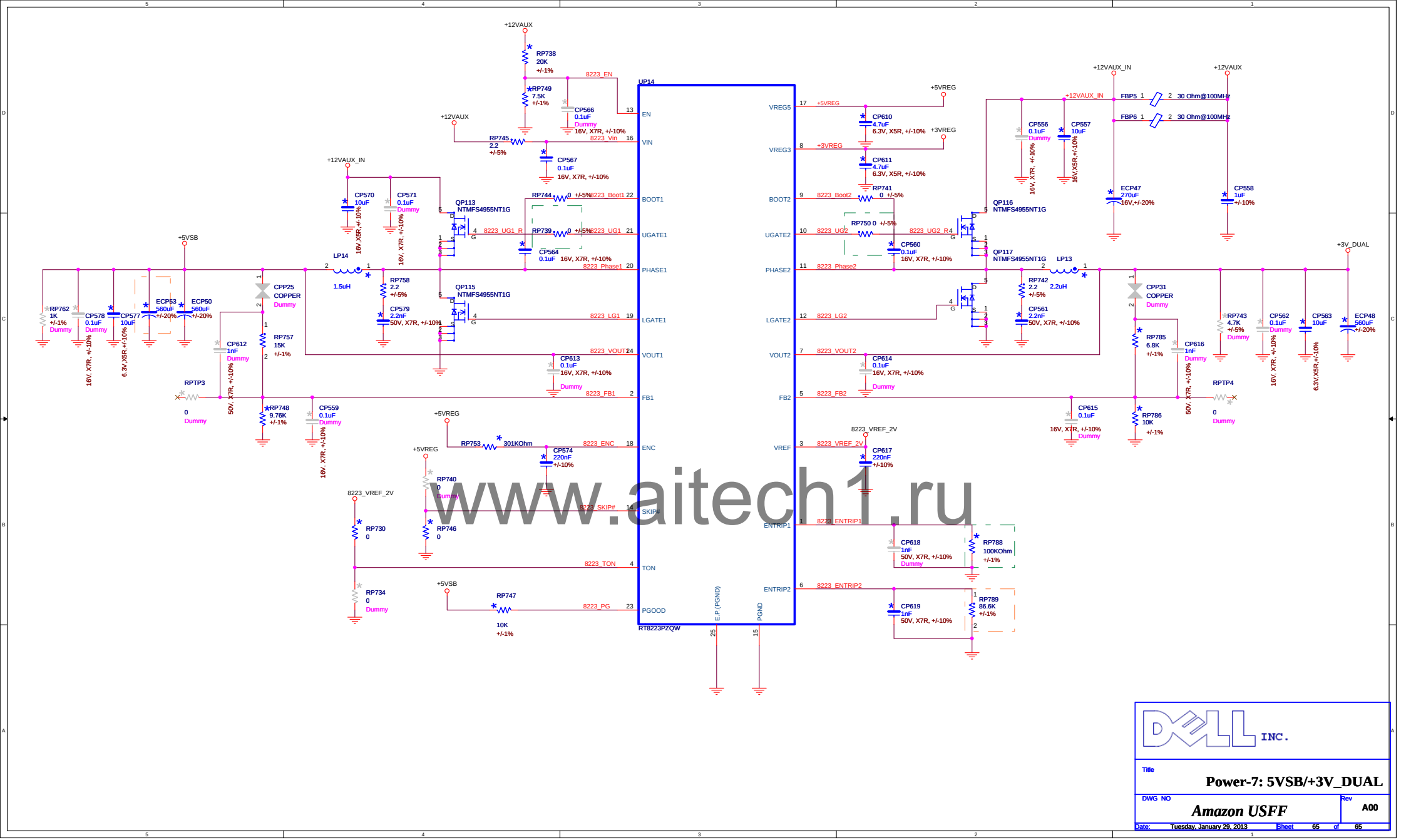

DELL INC.

Title: **Power-7: 5VSB/+3V_DUAL**

DWG NO: ***Amazon USFF*** Rev: **A00**

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